GOMACTech 2025

Government Microcircuit Applications and Critical Technology Conference

PROGRAM

MICROELECTRONICS
Full Throttle

March 17–20, 2025

Pasadena Convention Center
Pasadena, California

www. gomactech.net

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WELCOME TO GOMACTech 2025

This year's conference theme is "MICROELECTRONICS Full Throttle," and our robust program supports this theme by bringing together collaborators and innovators engaging across United States Government initiatives such as the CHIPS and Science Act, the National Defense Authorization Act (NDAA), and other strategic engagements across the Department of Defense and Department of Commerce. These engagements seek to establish and ensure the long-term sustainability of US-based semiconductor microelectronics manufacturing. This year's conference focuses on the importance of critical partnerships through private sector investments to ensure synergy between commercial needs and those of the United States government. As GOMACTech 2025 highlights these collaborative networks, it also provides a venue where partnerships enable technology to move from concept to implementation, and to transition, which benefits our nation and our warfighters. This year's conference features a series of workshops and panels that provide insights on how to engage with venture capitalists and program offices, while developing dual-use technologies. As we move full throttle into the coming years, *GOMACTech 2025 seeks to fuel the rebirth of the microelectronics revolution in our nation*.

The conference starts on Monday, March 17, with our signature workshops. The first is our annual Trusted Suppliers Industry Day, designed this year to address important changes since last year's Industry Day. The CHIPS Program office has accelerated funding for projects under the CHIPS and Science Act for the construction, expansion, or modernization of commercial facilities for the fabrication of leading-edge, current-generation, and mature-node semiconductors. DoD under the new administration will be examining and evaluating its approach to a microelectronics strategy and securing access to assured semiconductor supply chains. Monday also features two additional workshops: On Shore Advanced Packaging Capabilities Part Two, which presents technical overviews of currently funded on-shore advanced packaging efforts; and From Idea to Impact Workshop: Navigating the Startup Ecosystem, designed to empower emerging tech entrepreneurs by exploring how startups can commercialize cutting-edge technologies that not only disrupt markets but also enhance national security.

Our Monday programming will conclude with a welcome reception in the Conference Building Foyer, which is open to *all* registered attendees. Please join us!

GOMACTech 2025 formally opens on Tuesday, March 18, with an outstanding morning plenary session that includes keynote addresses from Mr. Roger Griffiths, team principal, Andretti Formula E, Andretti Extreme E; and Dr. Whitney Mason, director of the Microsystems Technology Office (MTO). Mr. Griffiths' talk focuses on "Microelectronics Commons: The New Battleground of Global Motorsport," and Dr. Mason's presentation is titled "More than Microchips."

Our 2025 Jack S. Kilby Lecture speakers are Ms. Deirdre Hanford, chief executive officer & trustee with Natcast, speaking on "The NSTC: Leveraging Public-private Partnerships to Advance U.S.-led Semiconductor R&D, Workforce, and National Security," and Dr. Carl McCants, special assistant for microelectronics policy at DARPA, whose presentation is titled "DoD Microelectronics – Transitioning Innovation in 2025 and Beyond."

This year the plenary session will also feature a special threat brief presentation from Mr. Adam Hauch of the Global Deterrence & Defense Department with Crane Division, Naval Surface Warfare Center (NSWC Crane).

In 2025, we are hosting seven panel discussions: “Global Chip Traceability: Securing the Semiconductor Supply Chain for a Resilient Future,” “Microelectronics Transition Activities/Challenges within Program Offices,” “Workforce Development and Mentorship,” “Microelectronics Innovation – Strategies for Dual-Use Applications in US Government,” “T&AM MPW Program,” “USG Microelectronics Advanced Packaging Landscape,” and “California DREAMS Hub/ MOSIS 2.0.”

The plenary, technical, and topical sessions are the major venues for information exchange at the conference, to help the community understand microelectronics and semiconductor investments, needs, and transition opportunities. Other opportunities for technical interaction are provided by the exhibits program, which includes major semiconductor, integrated circuit, and packaging manufacturers and commercial vendors of devices, equipment, software, intellectual properties, systems, and services for nearly every facet of the electronics business. The exhibition opens on Tuesday, March 18, at noon, and runs through Wednesday, March 19, at 4:00 pm. On Tuesday evening, all attendees can network in a relaxing atmosphere during the Exhibitors’ Reception.

Wednesday evening, March 19, features the Evening Social, held this year at The Wizarding World of Harry Potter at Universal Studios in Hollywood. In addition to the usual GOMACTech hospitality, including dinner and drinks, GOMACTech attendees will have exclusive use of this area of the park from 7 pm to 10 pm. The event starts with a Universal Studios tram tour at 6 pm, not to be missed! This ticketed event will have an attendance cap; therefore, if you are planning on attending, please buy your ticket via GOMACTech registration before Wednesday.

On Thursday morning, March 20, a poster session that includes our annual student poster competition will take place. The poster session is an opportunity for direct networking with the researchers on critical topics that affect the United States government.

This year’s technical program is a result of the hard work and enthusiasm of the GOMACTech 2025 Technical Program Committee. The committee members discussed and collaborated on the technical topic areas, sessions, and presentations. The quality of the conference reflects this comprehensive team effort. We hope that you find GOMACTech 2025 an enlightening, rewarding, and enjoyable experience. Thank you for your active participation.

Vipul J. Patel
Honorary General Chair

Wayne Churaman
Army Research Laboratory
Technical Program Chair

ABOUT GOMACTech

GOMACTech was established primarily to review developments in microcircuit applications for government systems. Established in 1968, the conference has focused on advances in systems being developed by the Department of Defense and other government agencies and has been used to announce major government microelectronics initiatives such as VHSIC and MIMIC, and to provide a forum for government reviews.

GOMACTech 2025 provides a forum for discussing and demonstrating advanced microelectronics and microsystems that can provide the means to develop confidence in transformational, leap-ahead technologies, and capabilities. GOMACTech is the premier forum for reporting on government-funded microcircuit research and other research efforts that focus on the technology needs of government systems.

REGISTRATION

All sessions at GOMACTech 2025 will be held at the Pasadena Convention Center. Both check-in and on-site registration will take place in the Ballroom Foyer of the Convention Center.

Conference check-in and on-site registration hours:

March 17	Monday:	7:00 AM – 6:00 PM
March 18	Tuesday:	7:00 AM – 5:00 PM
March 19	Wednesday:	7:00 AM – 5:00 PM
March 20	Thursday:	8:00 AM – 3:00 PM

Photography and any recording are *NOT* permitted in sessions or exhibit hall.

SECURITY PROCEDURES

GOMACTech is an unclassified, export-controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants, including presenters and exhibitors, must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, all attendees will be required to complete and sign non-disclosure agreements (NDAs) on site.

You may prove U.S. citizenship with any of the following:

- U.S. Passport
- Birth certificate AND valid government-issued photo ID
- Naturalization certificate AND valid government-issued photo ID
- Permanent resident card

The following cannot be used on their own as proof of citizenship:

- Voter registration card
- Driver's license

GOMACTech 2025 WORKSHOPS

Trusted Supplier Industry Day

Monday, March 17
8:00 am–5:00 pm
Room 107, Conference Building

The 15th Trusted Supplier Industry Day will be an interactive event with an opportunity for attendees to hear from key leaders and provide input on the critical issues facing our community. We have seen important changes since last year's Industry Day. The CHIPS Program office accelerated funding for projects under the CHIPS and Science Act for the construction, expansion, or modernization of commercial facilities for the fabrication of leading-edge, current-generation, and mature-node semiconductors. DoD under the new administration will be examining and evaluating its approach to a microelectronics strategy and securing access to assured semiconductor supply chains. The Industry Day program will feature speakers who will address evolving microelectronics strategies, with a focus on innovation, security, and integrity. Speakers will also address work being done by the Trusted Supplier community to assess unification and collaboration in end-to-end trust, value propositions and approaches to trusted FPGA's and third-party intellectual property. The Industry Day is being designed to provoke thoughtful conversations and up-to-date information on the many activities being pursued to restore U.S. leadership in semiconductor manufacturing with a semiconductor supply chain that considers security along with technical performance. Please join us on March 17th to add your voice to the discussion of the most critical electronics issues of the day.

On-Shore Advanced Packaging Capabilities Part Two

Monday, March 17
8:00 am–12:00 pm
Room 105, Conference Building

The government teams will present technical overviews of currently funded on-shore advanced packaging efforts including Reshore Ecosystem for Secure Heterogeneous Advanced Packaged Electronics (RESHAPE), Defense Production Act Investment (DPAI), and DARPA Next Generation Microelectronics Manufacturing (NGMM) teams. Program overviews, interactive discussions, and presentations from vendors on their advanced packaging manufacturing capabilities will provide an opportunity for attendees to hear from key stakeholders and provide input on the critical issues facing the advanced packaging community. Awards have been made through the Industrial Base Analysis and Sustainment (IBAS) program, RESHAPE effort, to Osceola County Fl/Skywater/BRIDG and Micross Components. The DPAI program has awarded Calument and GreenSource Fabrication LLC. The T&AM State of the art Heterogeneous Integrated Packaging (SHIP) program awarded SHIP RF to Qorvo. Speakers will address key needs and developments in packaging to include Fan-Out Wafer Level Packaging (FOWLP), Wafer Prep and High-Density Interconnent/High Density Build-up (HDI/HDBU). Please join us on the afternoon of March 18th to hear the latest in government packaging capability investments and be part of the needs and challenges discussions for this advanced packaging community.

From Idea to Impact Workshop: Navigating the Startup Ecosystem

Monday, March 17
1:30–4:30 pm
Room 104, Conference Building

Co-organized by Intel Capital, IQT, and GOMACTech

In a rapidly evolving technological landscape, startups are a key driving force behind innovation and in enabling the U.S. Department of Defense's (DOD) technical leadership. This half-day workshop is designed to empower emerging tech entrepreneurs by exploring how startups can commercialize cutting-edge technologies that not only disrupt markets but also enhance national security. Participants will gain insights into commercializing and scaling promising microelectronics technologies, the VC funding ecosystem, and gaining traction within the defense ecosystem. Through expert panels, interactive networking sessions, and a startup-led panel, the workshop will focus on creating opportunities for startups to connect and expand upon relationships within the systems providers and include a set of startups showcasing their innovations and impact on the defense sectors. This workshop offers a unique opportunity to connect with like-minded investors, innovators, industry leaders, and potential collaborators, to help drive forward the next generation of technology. The workshop will include talks introducing VC relative to GOMAC technology, partnering with VCs for Growth, a Q&A around advancing technologies for commercialization, a panel dedicated to discussing funding opportunities for commercialization, and startup presentations, following by a networking reception hosted by Intel Capital. Speakers and Panel Participants include and are not limited to Intel Capital, IQT, Booz Allen Hamilton, USC, and Lockheed Martin Ventures.

GOMACTech 2025 PANEL DISCUSSIONS

All panels take place in Room 107, Conference Building

Global Chip Traceability: Securing the Semiconductor Supply Chain for a Resilient Future

Wednesday, March 19
10:30 am

The Semiconductor Traceability and Market Provenance (STAMP) initiative aims to deliver traceability of every semiconductor and its capabilities through the supply chain to help deliver assured supply for critical infrastructure and economic security. This panel session will focus on the global chip traceability initiative, a critical development aimed at securing the semiconductor supply chain and enhancing its transparency, security, and resilience. Given the complexities of the global chip ecosystem and the growing geopolitical tensions, this session will explore the role of Global Chip IDs and their application in preventing counterfeiting, securing infrastructure, and ensuring export control compliance. Panelists will discuss the economic value created by chip traceability, the integration of lifecycle management tools, and the formation of cross-border public-private partnerships (PPPs) to support a scalable solution. The conversation will be grounded in how this aligns with the US and EU CHIPS Acts, and broader international cooperation efforts.

Microelectronics Transition Activities/Challenges within Program Offices

Wednesday, March 19
1:30 pm

Microelectronics transition is one of the greatest hurdles for any microelectronics development effort. This panel seeks to discuss topics related to the activities, challenges, and successes of microelectronics transition into program offices. Topics will include: use of tools for microelectronics digital engineering best practices, hardware and software co-development/testing/evaluation, and microelectronics integration into program roadmaps; to include, transition on-ramps, planning for upgradeability, obsolescence mitigation strategies that don't include life-time buys, contracting, deliverables, technical data packages, and more. This panel will include government program office and industry perspectives. The goal of this panel is to fuel community discussions with program offices on how to enhance and accelerate transition of microelectronics.

Workforce Development and Mentorship

Wednesday, March 19
3:30 pm

The semiconductor industry is facing a significant shortage of skilled workers, prompting numerous workforce development initiatives. To make a sustainable impact, it's crucial to focus on other steps, including effective mentorship programs. Mentorship can be a critical component of workforce development, providing individuals with the tools and guidance needed to succeed and remain in the industry. However, challenges such as being intentional in mentorship efforts and matching mentors with mentees effectively must be addressed. This panel will explore the mentoring process, discussing both the positive aspects and the challenges. Panelists will highlight the top three successes and difficulties in this area.

Microelectronics Innovation – Strategies for Dual-Use Applications in US Government

Thursday, March 20
8:30 am

Given the diminishing pace of progress correlated with Moore's Law, a variety of new computing technologies have emerged, including analog processing, stochastic/probabilistic methods, neuromorphic architectures, quantum systems, and 3D integrated circuits. These technologies have the potential to provide significantly greater computational power while adhering to size, weight, and power (SWaP) constraints. However, they are frequently constrained to specific applications and face significant challenges requiring specialized architectures, software support, and integration with existing systems. To achieve meaningful impact with these innovative technologies, it is essential to engage in co-design across multiple domains, including materials, devices, architectures, algorithms, and systems. The complexity of these challenges means that many promising technologies struggle to gain widespread commercial viability and sustainability. Relying on a single application from the US Government (USG) is not enough to mature and sustain these emerging technologies. To address this issue, we need both technical and policy solutions that foster the development of technologies with a viable commercial market. This will ensure their sustainability while also meeting mission requirements. This panel will bring together experts from academia, national laboratories, commercial sectors, and government agencies to explore how the academic and USG communities can collaboratively advance emerging computing technologies for dual-use applications.

T&AM MPW Program

Thursday, March 20
10:30 am

The Trusted and Assured Microelectronics (T&AM) Program within OUSD Research & Engineering (R&E) aims to provide the U.S. warfighter with the State-of-the-Art (SOTA), assured microelectronics required to meet DoD system modernization goals. One of the primary objectives of the program is to enable access to commercial industry to develop and demonstrate SOTA designs that advance DoD initiatives. T&AM sponsors Multi-Project Wafer (MPW) run opportunities to enable access to SOTA US commercial foundries ≤14 nm in support of the DoD microelectronics goals and to aid in developing DoD specific PDK's and IP. Currently, T&AM sponsors MPW opportunities with Global Foundries and Intel Foundry Services. The program is available to relevant designs from the defense industrial base (DIB), gov't labs, and academia. The panel will provide an overview of T&AM MPW opportunities and a discussion of technologies currently sponsored.

USG Microelectronics Advanced Packaging Landscape

Thursday, March 20
1:30 pm

The performance demands of defense and commercial applications alike continue to drive innovation in microelectronics development, pushing Moore's Law to the limit. At the same time, the need for high-performance, low-power compute across the electromagnetic spectrum calls for diverse solutions. Meeting the performance demands for these next generation systems requires significant innovation across the ecosystem. Complementary U.S. Government (USG) initiatives, such as DARPA's Next-Generation Microelectronics Manufacturing (NGMM) program, are driving this innovation through advanced packaging, with a focus on national security. This panel will bring together leaders from active USG microelectronics programs working toward both near-term and over the horizon advances, to facilitate a conversation with the USG microelectronics community around their respective challenges and goals.

California DREAMS Hub/MOSIS 2.0

Thursday, March 20
3:30 pm

MOSIS 2.0 is the primary operational entity of *CA DREAMS* – the Southern California-based superhub of the Microelectronics Commons program. Fully launched in 2024, MOSIS 2.0 integrates the facilities of 3 DIB full-flow compound semiconductor fabs and 7 university nano-fabs. A multi-faceted engineering staff has been assembled that supports the full range of MPW-related and nano-fab process R&D projects within the hub but also supports prototyping in other hubs' facilities and commercial foundries. This panel has two purposes: First is to provide a brief introduction to MOSIS 2.0, its operation, range of services, and status to the microelectronics community represented by the audience. The second purpose is to provide the R&D community with the opportunity to discuss and provide input that will help MOSIS 2.0 refine, balance, and potentially expand its capabilities. To this end a panel of experts representing different stake-holder elements of the micro-electronics R&D community will present their perspectives on the best way to optimize the accelerating impact of MOSIS 2.0.

GOMACTECH 2025 CO-LOCATED EVENTS

Room 104

Intel18A Technology: The DIB Design Experience

Wednesday, March 19
10:30 am

The intent of the panel is to discuss Intel18A technology and the experience of four DIB companies in using the technology to design test chips as part of the RAMP-C Program. Intel provides an introductory overview of the technology as context for presentations by the DIB companies. Boeing and Northrop Grumman discuss their experience using the Intel18A design ecosystem to design multiple Intel18A test chips that include digital and mixed-signal circuit blocks. Trusted Semiconductor Solutions and Reliable Microsystems discuss their recent experience on-boarding with the design-stable Intel18A PDK and its associated design collateral. The panelists then field questions from the audience regarding the presentations and the Intel18A DIB design experience.

A Department of Defense (DoD) Microelectronics Roadmap

Wednesday, March 19
1:30 pm

A comprehensive DoD microelectronics roadmap would align investments among the services, increase supply chain resiliency, and ensure long-term strategic planning. Microelectronics are foundational to DoD weapon systems, communications platforms, intelligence capabilities, and more; a roadmap would help mitigate risks associated with foreign dependence and supply chains while promoting collaboration among the defense sector, industry, academia, and our allies. The DoD must anticipate and invest in emerging technologies to maintain the competitive edge over our adversaries; a roadmap would create milestones for innovation and drive government-wide adoption for security and performance standards in microelectronics. While DoD participates and contributes to industry and academic oriented roadmaps, there is increasingly a need for us to coordinate internally to maximize the efficacy of our research investments and the interoperability of our systems. Additionally, the roadmap would inform intellectual property protections, workforce development initiatives, and export controls. This DoD microelectronics roadmap is essential to maintain technological superiority, secure the supply chain, and guide investments effectively.

Commercial-Scale Modernization of Defense Microelectronics

Thursday, March 20
10:30 am

Defense microelectronics deployment to the warfighter has well-understood challenges in access to state-of-the-art. However, prototyping, acquisition, and technology refresh is siloed across DoD components, causing reuse inefficiency and supply chain limitations in a highly disaggregated defense market for low-volume/high-mix solutions. Aggregating tri-service capabilities would increase volume and offer lower-mix common platform approaches. Further, the overall cost of supply chain development infrastructure is reduced with enterprise solutions. Lastly, enhanced methodology best practices to improve reliability become viable with such an approach. This would lift the caliber of the defense microelectronics industry and workforce to rival that of commercial electronics.

Speakers from government and industry will weigh in on novel approaches toward this goal.

LUNCHES

Lunches will be provided in the Exhibit Hall Tuesday through Thursday.

Supported by:

TRUSTED SUPPLIER OPENING NETWORKING RECEPTION

Sunday March 16
6:00–8:00 pm
Exhibit Hall B Foyer

We are pleased to hold a special get-together with the Trusted Supplier Industry Networking Reception on Sunday evening. Please join us for some food and drinks, meet your industry friends and colleagues, and relax before Monday's full agenda begins.

All GOMACTech 2025 registrants are invited to the Sunday evening reception.

WELCOME RECEPTION

Monday March 17
5:00–7:00 pm
Conference Building Foyer

Sponsored by:

All registered attendees are encouraged to join us for the opening reception.

WEDNESDAY EVENING SOCIAL

Offsite Evening at The Wizarding World of Harry Potter™
6:00–10:00 pm
Wednesday, March 19

Please join us for a legendary evening at Universal Studios, where The Wizarding World of Harry Potter will be reserved for GOMACTech attendees. Transportation will be provided to and from the event beginning at 5:30 pm and ending at 10:30 pm. Tickets are $75 per person and space is limited. Tickets must be purchased at registration prior to the event.

EXHIBITION

An exhibition made up of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are encouraged to visit the exhibition when they have some free time. The exhibition will be located in Exhibit Hall A&B. Coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening, March 18, an Exhibitors' Reception, where attendees can mix in a relaxing atmosphere with food and good spirits, will be held from 6:00 to 8:00 pm.

Exhibition hours are as follows:

Tuesday, March 18 – 12:00 pm – 8:00 pm
Wednesday, March 19 – 9:00 am – 4:00 pm

List of Exhibitors

3D Glass Solutions, Inc.
AAA Test Lab
AARD Technology LLC
Accurate Circuit Engineering
AdTech Ceramics
Advent Diamond, Inc.
Akoustis
Alphacore, Inc.
Altera, an Intel Company
AMD
AmTECH Microelectronics
Analog Devices
Ansys
Astronics Test Systems
ASU
Avalanche Technology
BAE Systems
Battelle
Boeing
Braun Electronic Components LLC
Cadence
CAST
Checkpoint Technologies
Chip Scan
Codasip
CoolCAD Electronics
Cycuity
DMEA TAPO
DOD ATEA
Draper
Edaptive Computing, Inc. (ECI)
Eshylon Scientific
Evatec NA
Everspin Technologies
Extreme Waves
Falcon Electronics, Inc
Finetech
Frontgrade
Georgia Tech Research Institute
GlobalFoundries
Golden Altos Corp.
Graf Research Corp.
Honeywell Aerospace Technologies
HRL Laboratories LLC
IBM
Idaho Scientific
IEEE Computer Society
Instec, Inc.
Integra Technologies, Inc.
Intel Corp.
ISI
JEOL
JRC Integrated Solutions

JSTF – Jazz Semiconductor Trusted Foundry
Kansas City National Security Campus
Keysight
Knowles Precision Devices
Laser Thermal Analysis
LeWiz Communications, Inc.
MACOM
Menta eFPGA, Inc.
Mercury Systems
Micrcohip Technology
Micropac Industries, Inc.
Microsanj
Micross
MIT Lincoln Laboratory
MITRE
MMEC
Mosaic Microsystems
MOSIS 2.0 | California DREAMS | USC/ISI
Movellus
MRSI Mycronic
Nano OPS, Inc.
Natcast
NHanced Semiconductors, Inc.
Nimbis Services, Inc.
Noble Metal Services
Northeast Regional Defense Technology Hub (NORDTECH)
Northrop Grumman
NSA Cybersecurity Collaboration Center
NSWC Crane
Omni Design Technologies
onsemi
PacTech USA, Inc.
Palomar Technologies
Penn State Applied Research Laboratory – Electronics Manufacturing Center
Photronics, Inc.
PQShield
Qorvo
QP Technologies
QuickLogic Corp.
Radiation Test Solutions
RAITH America, Inc.
Rambus
Raytheon
Real Intent
Red Balloon Security
Remtec, Inc.
S-Cubed
S2MARTS
Secure Micro Technologies LLC
SecureFoundry
Shibuya Corp.
Siemens
SiFive
Silicon Assurance
Silitronics Solutions, Inc.
Silvaco, Inc.
SkyWater Technology
Spectral Design and Test, Inc.
SRI International
StratEdge Corp.
Synopsys
Tektronix CSO
Tenet3
Triad Micro Devices
Trusted Semiconductor Solutions Inc.
Trusted Strategic Solutions
Trymax Semiconductor Equipment BV
UF | Florida Semiconductor Institute
Vitruvian Lab
YES Tech
Zero ASIC

GOMACTECH 2024 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech 2024 will include the George Abraham Outstanding Paper Award, a Best Poster Paper Award, and a Best Student Poster Paper Award. Presentation of these well-deserved awards will take place during the Plenary Session on Tuesday morning in Ballroom D-E. The GOMACTech 2024 winners are as follows:

The George Abraham Outstanding Paper Award

"2 to 18 GHz High Efficiency Power Amplifier"

Steve Nelson, Dumitru Grecu, Danny Bryant, Rajah Vysyaraju, Chris Ison, Rajesh Mongia, Howard Sheehan

ENGIN-IC, Inc.

Research funded by AFRL.

Best Poster Paper Award

"Fieldable Integrated Photonics Systems Across the Spectrum"

Cheryl Sorace-Agaskar, Colin Bruzewicz, Patrick Callahan, John Chiaverini, Christopher Heidelberger, Dave Kharas, William Loh, Thomas Mahony, Ryan Maxon, Robert McConnell, Alexander Medeiros, Alkesh Sumant, Meghan Schuldt, Reuel Swint, Paul Juodawlkis

MIT Lincoln Laboratory

Rachel Morgan, Kerri Cahoy

Massachusetts Institute of Technology

Research funded by USD(R&E), DOE, NSF, DARPA

The Les Palkuti Best Student Poster Paper Award

"Comparing Analog CMOS Hopfield and Ising Networks on NP-hard Problems"

Pranav O. Mathews and Jennifer O. Hasler

Georgia Institute of Technology

SURVEY AND GIFT

We are asking all our attendees to complete a short online survey so we can learn how to improve our conference next year. The survey is available through a link in the mobile app and through a QR code scan that will be posted on signs at the conference. When you have finished taking the survey, make a screenshot of your confirmation/thank-you notice and bring it or your confirmation email to the registration desk to receive a gift as our thank-you for completing the survey. (Note: Paper versions of the survey are also available at registration on request. If you are filling out a paper survey, please do not fill out an online version and vice versa.)

PROCEEDINGS

The GOMACTech downloadable proceedings contain searchable versions of accepted papers for the conference. Previous GOMACTech Digests are available to qualified Defense Technical Information Center (DTIC) users.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech 2025 include: CHIPS Program Office, Defense Advanced Research Projects Agency, Defense Logistics Agency, Defense Microelectronics Activity, Defense Threat Reduction Agency, Department of Defense Agencies, Department of Homeland Security, Department of the Air Force, Department of the Army, Department of the Navy, Intelligence Advanced Research Projects Agency, National Aeronautics and Space Administration, National Institute of Standards and Technology, National Nuclear Security Administration, National Reconnaissance Office, National Security Agency

GOMACTech WEB SITE

Information on GOMACTech may be obtained through its web site at www.gomactech.net.

CONFERENCE ASSISTANCE

Anyone requiring assistance at GOMACTech 2025 should contact the conference coordinators at the registration desk or as below:

Mari Ramirez and William Klein
GOMACTech/PCM
729 7th Avenue, Suite 1402A
New York, NY 10019-6991
813-381-3667
mramirez@pcm411.com and wklein@pcm411.com

TUESDAY, MARCH 18
(All Pacific Daylight Time)

PLENARY SESSION

Tuesday, March 18, 2025, Ballroom D-E

Breakfast (7:00–7:45)

Color Guard and National Anthem (8:00–8:15)

Opening Remarks and Awards (8:15–8:45)

Vipul J. Patel
GOMACTech 2025 Honorary General Chair

Wayne Churaman
GOMACTech 2025 Program Chair

Keynote Address I (8:45–9:30)

Mr. Roger Griffiths

Team Principal

Andretti Formula E, Andretti Extreme E

Microelectronics Commons: The New Battleground of Global Motorsport

This insightful overview contemplates the progression and development of microelectronics in auto racing, ranging from the more traditional platform of INDYCAR racing into the rapidly growing, fully sustainable, and all-electric FIA Formula E World Championship. Learn from a leader in the motorsports industry about how involving regulations and increased technology integration has led to software development being the new trackside weapon, both on and off the racetrack..

Keynote Address II (9:30–10:15)

Dr. Whitney Mason

Director

Microsystems Technology Office (MTO)

More than Microchips

Since the invention of the transistor in 1947 and the integrated circuit in 1958, microchips have fueled scientific advancements, manufacturing innovations, and economic growth for most of the modern era. Today, DARPA's Microsystems Technology Office (MTO) will advance the next generation of microsystems to disrupt the underlying technology, disrupt current manufacturing, and create new markets. This disruption requires unique insight to discover fundamentally new ways of creating advanced circuits that will dramatically alter and exceed the current state-of-the-art in microsystems. This will involve using the power of light at the microscale in three dimensions with advanced photonics. It will involve harnessing quantum mechanical phenomena for sensors and computers that break traditional classical limits. It will involve developing a toolbox of organic and biological molecules and hybrid bioelectronics that will exploit living system phenomena and connect back to traditional microsystems. Finally, it will involve developing technologies to affordably, rapidly, and sustainably fabricate these and other microsystems to lead to a new domestic manufacturing ecosystem that will exploit commercial scaling and underpin strong domestic economic growth.

BREAK (10:15–10:30)

Threat Briefing (10:30–11:00)

Mr. Adam Hauch

Global Deterrence & Defense Department

Crane Division, Naval Surface Warfare Center (NSWC Crane)

This briefing will examine counterintelligence threats facing the semiconductor industry, including case studies that highlight real-world risks and vulnerabilities within the supply chain. Attendees will gain insight into emerging threats, tactics used by adversaries, and best practices for safeguarding critical technologies. Additionally, we will provide counterintelligence points of contact for U.S. semiconductor companies seeking further guidance and support.

Jack S. Kilby Lecture Series

Kilby Address I (11:00–11:30)

Ms. Deirdre Hanford

Chief Executive Officer & Trustee

Natcast

The NSTC: Leveraging Public-private Partnerships to Advance U.S.-led Semiconductor R&D, Workforce, and National Security

The National Semiconductor Technology Center (NSTC) is a public-private consortium established by the CHIPS and Science Act and is dedicated to semiconductor R&D in the United States. Operated by Natcast, the NSTC convenes industry, academia, and government from across the semiconductor ecosystem to address the most challenging barriers to continued technological progress in the domestic semiconductor industry, including the need for a skilled workforce. Natcast CEO Deirdre Hanford shares insights into the once-in-a-lifetime opportunity presented by the NSTC, its activities to-date, and its impact on innovation, workforce, and economic and national security.

Kilby Address II (11:30–12:00)

Dr. Carl E. McCants

Director

Special Assistant for Microelectronics Policy

Defense Advanced Research Projects Agency

DoD Microelectronics – Transitioning Innovation in 2025 and Beyond

In the March 2024 "National Strategy on Microelectronics Research" published by the Subcommittee on Microelectronics Leadership of the National Science and Technology Council[1], one of the four goals and objectives is "Create a Vibrant Microelectronics Innovation Ecosystem to Accelerate the Transition of Research and Development to U.S. Industry". This goal "is focused on the entire R&D landscape and presents strategies and actions to create a vibrant microelectronics innovation ecosystem to… support actions at each stage of the microelectronics technology development pathway… to build a virtuous cycle of microelectronics innovation."[2] The DoD faces unique challenges in developing, accessing, and utilizing microelectronics design, fabrication, packaging and assembly, characterization, and failure analysis capabilities needed to maintain and extend technological leadership in national security applications. This talk will explore the question "How should the DoD microelectronics ecosystem change to leverage and transition innovative capabilities that keep pace with or create the state of the art?"

[1]https://www.nitrd.gov/pubs/National-Strategy-on-Microelectronics-Research-March- 2024.pdf

[2]https://www.nitrd.gov/pubs/National-Strategy-on-Microelectronics-Research-March-2024.pdf, p. vi.

LUNCH (12:00–1:30)

Exhibit Hall

Note: Papers without abstracts are in most cases CUI restricted.

Session 1 **(TA2 – Emerging Technologies)**

UWBGS I: POWER

Tuesday, March 18 / 1:30–3:10 pm / Ballroom A

Chair: **Robert Kaplar**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Andrew Green**
Air Force Research Laboratory, Wright-Patterson AFB, OH

1.1: ARPA-E ULTRAFAST Program Overview and Status **(1:30)**

Eric Carlson, Igor Cvetkovic, Chelsea Haughn
Booz Allen Hamilton, Washington, DC

Olga Blum Spahn
Advanced Research Projects Agency - Energy (ARPA-E), U.S. Department of Energy, Washington, DC

1.2: DOE BES ULTRA EFRC Program Overview and Status **(1:50)**

Robert Nemanich
Arizona State University, Tempe, AZ

1.3: Advances for Next-Generation Electronics: Establishing a Domestic Source of 150 mm Ga_2O_3 Substrates **(2:10)**

Drew Haven, David Joyce, John Frank
Luxium Solutions, Milford, NH

Robert Lavelle, Luke Lyle, David Snyder, William Everson, Daniel Erdely, Lance Gonzalez, Scott Pistner, Samuel Hallacher, Shawn Watkins
Pennsylvania State University Applied Research Laboratory, University Park, PA

Katherine Burzynski
Air Force Research Laboratory, Wright-Patterson AFB, OH

1.4: CLAWS Hub Overview and Status Update **(2:30)**

J. F. Muth, F. A. Kish, J. L. Jones
North Carolina State University, Raleigh, NC

The Microelectronics Commons program is a network of innovation Hubs and Core Facilities distributed across the United States all working toward a common goal of advancing domestic microelectronics technology discovery, innovation, and transition. The Commercial Leap Ahead for Wideband Semiconductors Hub (CLAWS) led by NC State University in Raleigh, North Carolina is focused on accelerating the development and transition of wide bandgap semiconductors with an innovative research foundry model and workforce development program with leading wide band gap companies that span the supply chain, defense industrial base partners, national laboratories and small companies. The technical focus has five main thrusts: Silicon Carbide Electronics, III Nitride RF Electronics, III Nitride Power Electronics, III Nitride Photonics, and Ultrawide Bandgap Electronics with the goal of building capability to address DOD needs and creating leap ahead technologies for civilian use.

1.5: Advancing Semiconducting AlN and its Alloys: Achievements, Challenges, and Future Prospects for High-Performance Devices **(2:50)**

W. Alan Doolittle, Habib Ahmad, Christopher M. Matthews, Sangho Lee, Keisuke Motoki, Emily N. Marshall, Paul Stephen Hutchinson Maltaghati
Georgia Institute of Technology, Atlanta, GA

BREAK **(3:10–3:30)**

ADVANCED PACKAGING RESEARCH AND INNOVATIVE TECHNOLOGY APPROACHES

Tuesday, March 18 / 1:30–2:50 pm / Ballroom B

Chair: **Daniel Radack**
Institute for Defense Analysis, Alexandria, VA

Co-Chair: **Vashisht Sharma**
Institute for Defense Analyses, Alexandria, VA

2.1: 3D Heterogeneous Integrated RF System-in-Package Using Glass Electronic Packaging (1:30)

Jeb H. Flemming, Ed Horne, Sheryl Miller, Rob Hulsman, Kyle McWethy, Craig Willis
3D Glass Solutions, Inc. (3DGS), Albuquerque, NM

3DGS presents a manufacturing platform for the production of vertically stacked glass substrates with heterogeneously integrated surface mount devices for advanced RF systems-in-package. This work includes the design, fabrication, and assembly of a true 3D Heterogeneously Integrated vertically assembled half-duplex 6–12 GHz Tx/Rx module using 4 stacked glass layers with 14 embedded components with excellent simulation vs. measurement agreement. Furthermore, we present early work on thermocycling environmental reliability test data and key design components (e.g. low loss 50Ω vertical interconnects) that produce low loss RF systems-in-packages. In this paper, we present design, production, assembly considerations that impact size, weight, and performance (SWAP) metrics for a variety of product definitions important to the US Defense community.

2.2: A Domestic Wafer-Level Heterogeneous System in Package Manufacturing Platform for National Advanced Packaging Needs (1:50)

Nicole Mueller, Andrew Goldfarb, Andrew Mueller
Draper, Cambridge, MA

Integrated Ultra-High Density (iUHD) is Draper's custom domestic packaging technology designed for heterogeneous integration (HI) of multi-sourced chips while minimizing package size, weight, and power (SWAP). iUHD is ideal for microsystems requiring reduced SWAP, enhanced functionality, reduced lengths of critical signals for SI/PI improvements, and performance in harsh environments. It leverages existing chip designs and known good die, allowing design flexibility (mix and match foundries, nodes, and materials) and quick-turn manufacturing process iterations not feasible in standard System on Chip (SoC) designs. iUHD fabrication occurs at Draper's Advanced Packaging Facility (APF) in St. Petersburg, FL, a Trusted Foundry that supports new design and process introduction as well as high manufacturing readiness level production. The APF is a 18K square foot ISO5 cleanroom facility that supports design, layout, packaging, assembly and testing of iUHD systems, from prototype to production, at unclassified and classified levels.

2.3: Release and Transfer of GaN Devices for Space Applications **(2:10)**

Owen Meilander, Mona Ebrish
Vanderbilt University, Nashville, TN

Lisa Sebastian
Rose-Hulman Institute of Technology, Terre Haute, IN

In this work, the heterogeneous integration of GaN high electron mobility transistors (HEMTs) through a micro-transfer printing process is demonstrated. A high (>95%) transfer success rate and limited device degradation after transfer was observed from multiple substrates to multiple adhesions layers including copper tape and KMSF 1000 photo-dielectric. Additionally, the viability of the adhesion layer for use in harsh environments was tested. No exfoliation or significant outgassing was observed when the sample was placed under a vacuum or when the temperature was varied from 8 K to 473 K. Finally, radiation testing is underway to further ensure the reliability of the transfer method for devices intended for space applications.

2.5: Thermally Enhanced mmWave TR Modules **(2:30)**

John Ditri, Dan Harris, Duc Huynh, Stephen Arfuso
Lockheed Martin Rotary and Mission Systems, Moorestown, NJ

David A. Swank, Matthew Walsh
Naval Surface Warfare Center, Crane Division, Crane, IN

BREAK **(3:10–3:30)**

ADVANCED RF COMPONENTS & DEVICES

Tuesday, March 18 / 1:30–3:10 pm / Ballroom C

Chair: **Lauren Pelan**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Christopher Coen**
Georgia Tech Research Institute, Atlanta, GA

3.1: A 9.05-to-18.5-GHz Octave-Tuning-Range VCO in 65 nm CMOS Achieving >192.3 dBc/Hz FoM (1:30)

Hao Guo, Taiyun Chi
Rice University, Houston, TX

We present an octave-TR VCO featuring (1) a new magnetic mode switching scheme that eliminates long interconnects between VCO cores, thereby increasing the tuning range (TR), and (2) a tuning-free, octave-BW common-mode resonator (CMR) for $1/f^3$ PN corner reduction and FoM improvement. The CMR also enables a 2f0 output. Combining f_0 and $2f_0$ outputs, we demonstrate 4.06:1 TR from 9.05 to 37 GHz, 190.7 dBc/Hz worst-case FoM, and 212.3 dBc/Hz worst-case FoMT with only 2.4 dB FoM variation across the TR.

3.2: Low-Loss mmWave and Terahertz Vanadium Dioxide Switches Using Photothermal Excitation (1:50)

David L. West, Nima Ghalichechian
Georgia Institute of Technology, Atlanta, GA

We present low-loss single-pole single-throw (SPST) switches based on photothermally excited vanadium dioxide (VO_2). VO_2 is a phase-change material that exhibits an insulator-metal transition at 68 °C, accompanied by an abrupt shift in conductivity by up to five orders of magnitude. This property enables the development of ultra-low-loss RF switches. Typically, dc micro-heaters are used to locally transition VO_2 switches, but such heaters introduce parasitic capacitance that impairs performance at mmWave and terahertz. To address this limitation, we propose photothermally exciting the phase transition of VO_2 using a laser. We have previously experimentally demonstrated photothermally excited VO_2 switches with <0.43 dB insertion loss and >17.7 dB return loss in the ON state and >17.2 dB isolation in the OFF state up to 65 GHz. Our second-generation switches have been simulated up to 325 GHz. Design, fabrication and measurement results will be presented at the meeting.

3.3: Vanadium Dioxide Energy Selective Surface as an External Limiter for Sensitive Receiver Protection (2:10)

Walter Disharoon, Sree Adinarayana Dasari, Nima Ghalichechian
Georgia Institute of Technology, Atlanta, GA

Joshua Kovitz
Georgia Tech Research Institute, Atlanta, GA

A novel vanadium dioxide (VO_2) energy selective surface was designed, fabricated, and tested for operation in X-band. VO_2 is an insulator-metal-transition phase-change material that exhibits a sharp conductivity change at a temperature of 68 °C or a large electric field. The periodic surface takes advantage of this nonlinear behavior of VO_2 to allow low-power waves to be collected but reject nearby in-band or near-in-band interference sources. The protection can result in a more robust receive chain for high-sensitivity receive systems. The energy selective surface has a 3-dB transmission bandwidth between 9.5–10.5 GHz, in the low power state, and a greater than 30-dB rejection (0.1% of power transmitted) in the high-power state.

3.4: High-Data-Rate VLF Magnetoelectric Communications with Single-Side-Band Nonlinear Antenna Modulation (2:30)

Yisi Liu, Thomas Noochan, Bin Luo, Mark Sun, Nian Sun
Northeastern University, Boston, MA

Mohan Sanghadasa
US Army DEVCOM Aviation & Missile Center, Redstone Arsenal, AL

Very Low Frequency (VLF) electromagnetic waves enable communication in water and earth. However, conventional electrical VLF antennas exhibit large size, high power, and suffer from low data rates (~200 bit/s). Recent advancements in Magnetoelectric (ME) antennas have reduced antenna size, but limitations in bandwidth and efficiency remain. In this work, we introduce Single-Side-Band Nonlinear Antenna Modulation (SSB-NAM) for VLF ME antennas, achieving higher signal-to-noise ratio (SNR), high data rates over 10 kb/s, and stronger output upper to 20 m compared to Double-Side-Band NAM. By adjusting the carrier frequency with baseband data, SSB-NAM provides robust, wide-bandwidth communication, demonstrating stable transmission performance across a 0.5–10 kHz range. This method enhances VLF communication for underwater and underground applications.

3.5: Trends, Challenges, and Opportunities of GaN Based High Temperature RF Electronics (2:50)

John Niroula, Qingyun Xie, Minsik Oh, Hridibrata Pal, Matthew A. Taylor, Can (Rachel) Jiang, Pradyot Yadav, Tomás Palacios
Massachusetts Institute of Technology, Cambridge, MA

Shisong Luo, Yuji Zhao
Rice University, Houston, TX

High temperature electronics is becoming increasing important due to rising applications in high temperature (250+°C). many of which are critical to national and military interests. Here we summarize, some important trends in high temperature gallium nitride (GaN) based electronics and demonstrate record performance of GaN transistors at 500 °C.

BREAK (3:10–3:30)

PROTECTION METHODS AND APPLICATIONS

Tuesday, March 18 / 1:30–3:10 pm / Ballroom D&E

Chair: **Mona Massuda**
Department of Defense

Co-Chair: **Gail Walters**
Parallax Advanced Research, Colorado Springs, CO

4.1: On the Applicability of Logic Locking for Protecting Sensitive Microelectronics **(1:30)**

Jason Hamlet, Jonathan Cruz
Sandia National Laboratories, Albuquerque, NM

John Haussermannn
National Security Agency, USA

4.2: Enabling Secure Optical Communication with Silicon-Photonic-Based Physical Unclonable Functions (PUFs) **(1:50)**

Ebadollah Taheri, Kaveh Rahbarbard Mojaver, Mahdi Nikdast
Colorado State University, Fort Collins, CO

Ensuring security in optical communication networks requires innovative and reliable authentication methods. This paper reviews our recent work on silicon-photonic-based Physical Unclonable Functions (PUFs) using Contra-Directional Coupler (CDC) devices to generate unique and unclonable keys. These CDC-based PUFs leverage fabrication-process variations to create complex and secure responses. Our designs include randomized corrugation and ring-assisted structures, and achieve an average Hamming distance of over 0.2 for authenticating devices. Experimental results show these PUFs' strong resistance to machine learning attacks, with a Hamming distance above 0.4 and a standard deviation under 0.01 across 10,000 challenge-response pairs. Our PUF offers a robust solution for optical systems, surpassing traditional electronic PUFs in security.

4.3: Process Attestation and Device Fingerprinting: A Digital-Centric Time-Based Sensor Exploiting Back-End-of-Line Resistance and Capacitance **(2:10)**

Jen-Chieh Hsueh, Michael Kines, D. Shane Smith, Waleed Khalil
Ohio State University, Columbus, OH

Jamin McCue, Brian Dupaix, Vipul J. Patel
US Air Force Research Laboratory, Dayton, OH

This paper introduces an innovative time-based sensor leveraging the inherent Back-End-Of-Line (BEOL) resistance and capacitance to provide die authentication, with the capability to enable die identification and tamper detection. To achieve this with minimal overhead, the proposed sensor employs a highly digital architecture, with over 80% of the layout synthesized using an Auto Place Route (APR) digital flow. Furthermore, a novel ring-based quantizer is proposed to enhance sensor resolution, addressing the challenge of measuring small time-constants directly. The time-based sensor is fabricated using a 22 nm Fully-Depleted Silicon-On-Insulator (FD-SOI) CMOS process, occupying an area of 2040 μm^2. Operating at a clock rate of 500 kHz and a supply voltage of 0.8 V, the sensor's consumes 2.77 mW. The measured results demonstrate a close alignment with simulations, verifying the effectiveness of the circuit.

4.4: High-Resolution 3D Imaging and Analysis of Semiconductor Chips using Ultrashort Pulsed Lasers, Correlative Imaging, and Synthetic Data **(2:30)**

Matthew Maniscalco, Hongbin Choi, Adrian Phoulady, Alexander Blagojevic, Toni Moore, Mohammad Taghi Mohammadi Anaei, Parisa Mahyari, Marcus Emanuel, Nicholas May, Sina Shahbazmohamadi, Pouya Tavousi
University of Connecticut, Storrs, CT

This study addresses the critical need for high-resolution 3D imaging of semiconductor chips for verification, validation, obsolescence management, and IP recovery. Traditional methods like non-destructive X-ray CT imaging lack the necessary resolution, while Focused Ion Beam (FIB) combined with Scanning Electron Microscopy (SEM) is prohibitively slow. We propose an innovative approach using ultrashort pulsed lasers for delayering combined with multiple imaging modalities to construct high-resolution 3D images efficiently. Post-imaging, these images require sophisticated analysis to extract GDSII and netlist information, a process traditionally demanding significant manual effort. We demonstrate the efficacy of using synthetic data to train machine learning algorithms for automated image analysis, significantly reducing manual labor and enhancing accuracy.

4.5: Exploring Fingerprinting Techniques based on the Output of Pluggable Optical Transceivers **(2:50)**

LeAnn M. Hamilton, Leonardo G. De Mesquita, Ryan J. Herrington, Stephen W. Howell
NSWC Crane, Crane, IN

BREAK **(3:10–3:30)**

DIGITAL I

Tuesday, March 18 / 1:30–3:10 pm / Ballroom H

Chair: **Abirami Sivananthan**
InQTel, Arlington, VA

Co-Chair: **Seyi Ayorinde**
Army Research Laboratory, Los Angeles, CA

5.1: Path to a Viable Chiplet Ecosystem (1:30)

Daniel W. Bliss
Arizona State University, Tempe, AZ

We discuss the barriers and potential paths to improving the viability of a chiplet ecosystem. During multiple system-on-chip (SoC) development projects, we considered implementing our SoCs as chiplets to increase flexibility post fabrication. Chiplets promise higher inter-chip data rates at lower power. For our projects, potentially interfacing to transceivers, analog-digital converters, memory, or backend data interface chips would be useful. However, multiple hurdles exist to broad acceptance. We discuss these hurdles and suggest some steps to develop a viable chiplet ecosystem.

5.2: Collaborative Pilot Program Assisting Multi-Project Wafer Execution (1:50)

Randy W. Mann, Eric Ebersole, Patricia Schaefer, Doug Palmer, Saverio Fazzari
BOOZ ALLEN HAMILTON, McLean, VA

Oluseyi A. Ayorinde
DEVCOM Army Research Lab, Adelphia, MD

The multi-project wafer (MPW) is critical in the development of new design IP for the DoD microelectronic ecosystem. The migration of DoD microelectronics to state-of-the-art (SOTA) technologies is essential to remain competitive globally. To optimize success in multi-project wafer (MPW) design cycle and tape-out execution, a pilot program is being developed to help improve efficiency and reduce program delays. This is accomplished through the collective insights gained through multiple collaborative engagements. This effort provides a framework for risk analysis and insights from learning across important government design efforts to assist MPW efforts relevant to the DoD.

5.3: Low SWAP High Frequency Reference Timing Chiplet (2:10)

E. Alban, B. Carlton, R. Dorrance, T. Huusari, R. Liu, H. Luo, J. Mix, R. Vidana Morales, S. Shahraini, K. Ridgeway, M. Abdelmoneum
Intel Corporation, Hillsboro, OR

R. Abdolvand
University of Central Florida, Orlando, FL

T. Olsson
University of Pennsylvania, Philladelphia, PA

G. Piazza
Carnegie Mellon University, Pittsburgh, PA

We present a ~1 GHz reference timing clock chiplet that can be ubiquitously used across commercial and defense system standards to enable more than 10× SWAP gain while domestically volume produced in the US. The developed high frequency reference clock demonstrated less than 60 fs of RMS jitter at less than 1.5 mW of power. Such reference clock delivers unprecedented performance required by massive data processing for Artificial

Intelligence workloads, as well as emerging needs for stable clocks to synchronize across massive number of systems in GPS denied environment. The developed chiplet achieves resilient performance under severe operational conditions that currently requires expensive measures to ensure functionality like radio frequency interference from wireless congested environments. The developed chiplet can be heterogeneously integrated in a variety of emerging packaging technologies either in simple 2D integration or 3D stacking or embedding in packaging substrate delivering additional obfuscation and protection against the external environment.

5.4: Third Party Intellectual Property: Report on Microelectronics Designs (2:30)

Saverio Fazzari, Patricia Schaefer, Kevin Farrell, Mark Vlassakis, Benjamin Luong
Booz Allen Hamilton, Arlington, VA

Booz Allen's study on third-party intellectual property (3PIP) in DoD microelectronics highlights usage, sources, market share, licensing issues, security benefits and risks, and the feasibility of security-certified 3PIP. Surveying over 20 organizations, the study found widespread 3PIP use with concerns about vendor verification, insufficient security risk guidance, and standardization issues. Licensing issues included high costs and delays due to limited negotiation leverage for DIBs. Security benefits of 3PIP included rapid vulnerability detection and stringent development processes, while risks involved provenance and verification challenges. DIB-developed IP offered better verification visibility and customization but faced higher functional risks and limited infrastructure. Establishing a collection of security-certified 3PIP is feasible with a dedicated government organization to standardize agreements, verification processes, and maintain a central IP repository.

5.5: Unlocking PPA Benefits of Intel 18A Backside Routing (2:50)

Ashish Khurana, Augustine Weaver
Synopsys, Inc, Sunnyvale, CA

The power delivery network is a critical part of any modern semiconductor device. Traditionally, power was distributed through metal layers on the same side of the substrate as the signal metal layers where they competed for routing resources. A more optimal power distribution strategy is to power transistors from the backside of a wafer. A backside power delivery network improves performance, power and area (PPA) by addressing IR droop, increases density through additional cell shrinkage, and reduces congestion on the frontside. This paper presents a study that showcases how Synopsys and Intel Foundry collaborated to demonstrate the Intel PowerVia backside routing technology on the 18A process and will present data on wirelength, routeability, wire density, cell density, power and thermal with top-level clock tree network and critical signals in the backside layer stack. Backside routing solutions enable next-generation high-performance, AI, Automative, Mobile and hyperscaler application chips.

BREAK (3:10–3:30)

RADIATION HARDENED TECHNOLOGIES AND SYSTEMS

Tuesday, March 18 / 1:30–3:10 pm / Ballroom G

Chair: Pauline Paki
DHS Science and Technology, Washington, DC

Co-Chair: Hugh Barnaby
Arizona State University, Tempe, AZ

6.1: Modular Cryogenic System for Radiation-Hardened Device Testing (1:30)

Payton Muscat, Jereme Neuendank, Hugh Barnaby
Arizona State University, Tempe, AZ

Manny Teran, Chris Foster, Jake Roberts
IRLabs, Tucson, AZ

The IRLabs Rigel Dewar Insert for Static Temperature (DSTAT) system is a radiation-hardened device characterization system that allows for simultaneous radiation at cryogenic temperatures. The system enables data collection on total ionizing dose (TID) effects from temperatures ranging from 300 K to 77 K. The modular focus of the system allows for any device package to be tested, with current setups focusing on dual in-line packages (DIP) and leadless chip carriers (LCC). By interfacing with a programmable switching matrix and a Keysight B1500A, countless characterization programs can be created and ran for any type of device remotely. Initial results demonstrate its effectiveness in capturing TID-induced degradation with a large signal to noise ratio (SNR) while maintaining cryogenic temperatures for upwards of 7 hours. Future revisions while focus on expanding the temperature range, improving automation, and integrating additional measurement instruments to improve precision and accuracy.

6.2: Scalable Ferroelectric Nonvolatile Memory for Harsh Environment Applications (1:50)

Chloe Leblanc, Dhiren K. Pradhan, Shun Yao, Roy H. Olsson III, Deep M. Jariwala
University of Pennsylvania, Philadelphia, PA

David C. Moore, W. Joshua Kennedy, Nicholas R. Glavin
Air Force Research Laboratory, Dayton, OH

High-temperature and radiation-resistant non-volatile memory (NVM) is critical for advanced electronics operating in extreme environments. Numerous emerging applications including aerospace, space exploration, and nuclear plants require complex computing and sensing capabilities under harsh conditions, such as high temperatures and high levels of radiation. Ferroelectric $Al_xSc_{1-x}N$ exhibits strong potential for utilization in NVM devices operating at very high temperatures (>600 °C) and exposure to high levels of radiation given its stable remnant polarization (PR) and high ferroelectric transition temperature (TC) >1000 °C. Here, we demonstrate an $Al_{0.68}Sc_{0.32}N$ based ferrodiode NVM that can reliably operate at up to 600 °C over 1 million read cycles and readable On-Off ratio above 1 for >60 hours. Its operating voltage (<15 V at 600 °C) is compatible with existing Silicon Carbide (SiC) high T technology. In addition, these NVM devices maintain their polarization state throughout exposure to C60 gamma radiation, marking a significant step toward NVM technology for harsh-environment electronics.

6.3: An X-Band SiGe BiCMOS Direct-Conversion Receiver for Europa-Surface Missions **(2:10)**

Zachary R. Brumbach, Justin P. Heimerl, Jackson P. Moody, Delwyn G. Sam, James H. Shin, Brett L. Ringel, Donald H. Bailie, John D. Cressler
Georgia Institute of Technology, Atlanta, GA

Jeffrey W. Teng
The Aerospace Corporation, El Segundo, CA

Benjamin J. Blalock
University of Tennessee, Knoxville, TN

Gregory R. Allen, Dennis O. Thorburn, Linda Del Castillo, Bernard G. Rax, Mohammad M. Mojarradi
California Institute of Technology, Pasadena, CA

Europa lies in Jupiter's colossal radiation belt, producing radiation surface conditions that are so severe (5 Mrad[Si]) that most modern electronics would experience degradation in a matter of days. This challenge, coupled with the sub-100 K surface temperatures, leads to a very hostile environment for a viable electronic infrastructure. This paper describes a X-Band Silicon-Germanium BiCMOS direct-conversion receiver that is both total ionizing dose (TID) tolerant, and operates with enhanced performance at Europa surface temperatures.

6.4: Isolation of the STI Structure and its Response to Ionizing Radiation **(2:30)**

Tyler Kirby, Ching-Tao Chang, Hugh Barnaby
Arizona State University, Tempe, AZ

This paper describes the development of shallow trench isolation (STI) radiation test devices. The STI device variant is composed of multiple structures that enable total ionizing dose (TID) analysis for advanced CMOS technologies across fabrication process variables. A factorial design study will be performed with these devices to determine which process conditions best mitigate TID effects.

6.5: Fast, Low Risk, State-of-the-Art Rad Hard Mixed Signal Development **(2:50)**

Thomas L. Wolf, Kent F. Smith, Whitney Durham
Silicon Technologies, Inc., Salt Lake City, UT

State of the art electronics systems use analog and mixed signal microelectronic sensors, wireless communications, video, audio, radar, GHz data transmission, clocks, and other critical circuits. The Intel 16 and GlobalFoundries 12 nm processes offer tremendous advantages for system performance. Unfortunately, the design of such circuits is complex and time consuming. Further, when product requirements require radiation tolerance, the design cycle balloons. The ADONISTM Correct by Construction Technology integrated with Reliable Microsystems Radiation Models provides a silicon verified method to improve the most time consuming tasks of design, simulation, layout, verification, and radiation tolerance modeling. In this talk, we discuss the latest radiation silicon test results on both the Intel 16 and GF12 ADONIS chips. Supporting two of the three major EDA vendors.

BREAK **(3:10–3:30)**

UWBGS II: RF

Tuesday, March 18 / 3:30–5:30 pm / Ballroom A

Chair: **David Meyer**
Naval Research Laboratory, Washington, DC

Co-Chair: **Tony Ivanov**
Army Research Laboratory, Adelphi, MD

7.1: **ARO Ultra-Wide Bandgap RF Electronics Center: Overview and Status** **(3:30)**

Tom N. Oder, Joe X. Qiu
DEVCOM ARL Army Research Office, Durham, NC

7.2: **DARPA LADDIS Program Overview and Status** **(3:55)**

Todd Bauer
DARPA, Arlington, VA

7.3: **<100> Homoepitaxial Diamond Metal-Insulator-Semiconductor Schottky Diodes Towards High-Power RF Limiters** **(4:20)**

Brian Bersch, Noah Sauber, Thomas Adam, Brant Hempel, Alec Federice, Victor Hu, Nathaniel Rogers, Harlan Cramer, Bettina Nechay, Michael Marakovits, Sara Taylor, Ugonna Ohiri , Robert Howell, Matthew Doerflein, Josei Chang
Northrop Grumman Mission Systems, Linthicum, MD

7.4: **Applied Research for the Advancement of Science & Technology Priorities Program: Building Enduring Technical Capabilities Across the Department of Defense Laboratories** **(4:45)**

Karl J. Dahlhauser
Office of the Assistant Secretary of Defense (Science and Technology), Washington, DC

7.5: **UWBGS Panel Discussion** **(5:10)**

UWBGS Panelists
RF Session, Pasadena, CA

ADVANCES IN MODELING FOR PACKAGE DESIGN

Tuesday, March 18 / 3:30–5:10 pm / Ballroom B

Chair: **Mona Massuda**
Department of Defense

Co-Chair: **Marcia Sawhney**
Department of Defense

8.1: Enabling the Ecosystem of True Heterogeneous 3D IC Designs (3:30)

Anthony Mastroianni
Siemens DSIW, Annandale, NJ

Heterogeneous integration itself isn't new, but new design and manufacturing technologies, combined with new product demands from system integrators, means that heterogeneous integration and 3D IC are now becoming a necessity in mainstream design. This shift however is not without its challenges as 3D IC is not a simple extension of existing packaging solutions but creates a whole new set of multiphysics integration considerations. The interaction of thermal, mechanical, reliability, test, and core semiconductor design increases complexity and requires disparate domains to seemly collaborate. These challenges also require a new set of design enablement kits to support the heterogeneous supply chain in this new 3D IC codesign process. In this paper we explore the workflows, ecosystem and 3D IC Design Kits (3DK) which enable the design planning, implementation, verification and handoff to manufacturing of these new 3D IC heterogeneous designs.

8.2: Chiplets Modelling & Characterization for Disaggregated, Heterogeneous Integration (3:50)

Jamil Kawa
Synopsys, Inc., Sunnyvale, CA

Marco Casale-Rossi
Synopsys Italia Srl, Agrate Brianza, Italy

Dale Donchin
Synopsys, Inc., Marlborough, MA

Abstraction (which implies modelling, and characterization) has been the cornerstone of two revolutions in integrated circuits realization: polygon layout in the '80s, and logic synthesis in the '90s. We are at the dawn of another revolution: disaggregated (chiplet-based), heterogeneous (2.5D+ packaging) integration. The lack of a comprehensive modelling, and characterization solution may harm the adoption, and the deployment of chiplet-based systems.

8.3: ML-based 3D Floorplanning Solution for Multi-die System Thermal Integrity (4:10)

Lang Lin, Norman Chang
Ansys Inc., San Jose, CA

Jerome Toublanc,
Ansys Inc., France

Jie Yang,
Ansys Inc., Austin, TX

The Emerging 3D heterogenous integration (3DHI) technique has presented significant challenges and opportunities to EDA community, from 3D system floorplanning to reliable system signoff. In this paper, we first present an early-stage floorplanning flow to build a multi-die 3DHI system with power

assignment, chip thermal modeling and multi-die thermal simulation. Next, a fast and effective ML-based simulation methodology is demonstrated to achieve thermal-aware floorplanning at the 3DHI assembly stage.

8.4: An Integrated Approach to Advanced 2.5D/3D Package Thermal Design: Enhancing Collaboration and Efficiency (4:30)

Andras Vass-Varnai
Siemens EDA, Chicago, IL

Subramanian Lalgudi
Siemens EDA, Austin, TX

Tatiana Trebunskiskh
Siemens PLM, Frankfurt, Germany

Alex Strickland
Siemens EDA, Wilsonville, OR

Thermal management is crucial in modern microelectronic package design due to rising power densities and 3D heterogeneous structures. Traditionally, separate teams handle package design and thermal management, causing issues with integrating thermal models due to differing tools. This paper introduces two workflows to address this challenge. The first integrates a CFD-based solution directly into the chiplet and package design process, allowing for thermally driven floorplanning and creating a thermal digital twin of chip and package models, thus avoiding separate thermal model creation. The second workflow uses mechanical CAD (MCAD) for multi-physics simulation. It exports the package structure as an MCAD file, facilitating the addition of mechanical elements like stiffener rings or lids and enabling final multiphysics verification of complex cooling assemblies and potentially higher modeling accuracy of the interconnect system.

8.5: Power Delivery and Thermal Management of 3D Advanced Microsystem Assemblies (4:50)

John N. Damoulakis
Cadence Design Systems, San Jose, CA

Timothy Chainer
IBM Research, T.J. Watson Research Center, Yorktown Heights, NY

Ganesh Subbarayan
School of Mechanical Engineering, Purdue University, West Lafayette, IL

The 3D chips design challenges are presented and solutions proposed, supported by experimental results, to remedy them to produce thermally-reliable 3D microsystem assemblies. Approaches rely on the use of power delivery and thermal management EDA tools offered by Cadence Design Systems involving the Celsius studio and other. Fast multi-physics and multi-scale solutions, enabled by the tenets of artificial intelligence and machine-learning, are an integral part of approach. Mathematical models of critical challenges are discussed that are embedded in Cadence's thermal tools. But the approach provides, also, the required infrastructure for the thermal engineers to use their own models. An integrated interactive framework is proposed for power delivery and thermal modeling, which in-concert with models developed by the electrical, mechanical, and manufacturing engineers, is used to evaluate and quantify the thermal balance of 3D microsystems under various workload operating conditions. The enablement is based on the notion of the co-design paradigm.

Session 9 **(TA9 – RF Technologies, Components, and Systems)**

ALGORITHMS AND EDA TOOLS FOR MODELING, ANALYSIS & FABRICATION

Tuesday, March 18 / 3:30–5:10 pm / Ballroom C

Chair: **Mark Yeary**
Advanced Radar Research Center (ARRC) at the University of Oklahoma, Norman, OK

Co-Chair: **Nelson Lourenco**
Georgia Tech Research Institute - Sensors and Electromagnetic Applications Laboratory, Smyrna, GA

9.1: Co-design for Edge AI: Modulation Recognition (3:30)

John G. Wohlbier, Ralph Quartiano, Scott McMillan
Carnegie Mellon University, Software Engineering Institute AI Division, Pittsburgh, PA

Daniel Bonness, Chris Wible
Pennsylvania State University, Applied Research Laboratory, State College, PA

This paper presents the development of specialized accelerator intellectual property for Modulation Recognition systems in edge AI hardware optimized for size, weight, and power. Using High-Level Synthesis (HLS) for machine learning algorithms and manual Register Transfer Level coding for signal processing tasks like the Strip Spectral Correlation Algorithm (SSCA), we integrated accelerators into a system-on-chip (SoC) environment using the Embedded Scalable Platforms framework. The FPGA-based accelerators for ResNet and SSCA demonstrated performance gains of up to 20× compared to software implementations on conventional hardware. Future work includes optimizing the HLS flow for broader machine learning support, extending SoC integration to diverse workloads, and transitioning the accelerators into real-world defense applications. These efforts will enhance the performance and efficiency of edge AI systems in mission-critical environments.

9.2: Neural Network Terrain Correlation and Kalman Filtering for GPS-Denied Positional Awareness (3:55)

Kellie McClernon, Christopher Bennett, Daniel Ries, Sapan Agarwal, Tianyao Xiao
Sandia National Laboratories, Albuquerque, NM

9.3: In-Design Multiphysics Analysis for Validating and Mitigating Thermal Impacts (4:20)

Ken Mays
Boeing Research&Technology, Tukwila, WA

The ability to understand the thermal impact on performance has become a necessity for today's complex electronic designs. Having an integrated thermal analysis tool within a multiphysics system design flow proves to be very beneficial for determining overall performance and becomes necessary to maintain design flow synchronization. This paper demonstrates the capabilities of the Cadence Celsius Thermal Solver, an electrothermal co-simulation solution that provides analysis and design insights to detect and mitigate thermal issues early in the design cycle. Simulations are validated with measurements on devices designed for thermal imaging and current density performance.

9.4: AI-Assisted Design Automation for Digitally Controlled Oscillators (DCOs) with Two Examples Achieving >192.4 dBc/Hz FoM and <1.5 kHz Frequency Resolution (4:45)

Yaolong Hu, Hao Guo, Jiaqi Liu, Taiyun Chi
Rice University, Houston, TX

Shikai Wang
George Washington University, Washington, DC

Weidong Cao
George Washington University, Houston, TX

Leveraging AI-human collaboration, we decompose DCO design process into two steps and use design automation to enhance productivity and optimize performance in each step. The AI-assisted design flow features end-to-end synthesis in 80 seconds, generation of unconventional passives, frequency agility (1–20 GHz), and design robustness validation. The proposed DCO design automation is demonstrated using two examples, achieving >192.4 dBc/Hz FoM and <1.5 kHz frequency resolution at 7.1–8.6 GHz and 3.8–4.6 GHz.

TESTING AND VERIFICATION

Tuesday, March 18 / 3:30–5:10 pm / Ballroom D&E

Chair: **Adam Duncan**
NSWC Crane, Crane, IN

Co-Chair: **Kelsey Bramschreiber**
NSWC Crane, Crane, IN

10.1: Expanding the Application of Dynamic Reconfiguration Through Advanced Approaches to Independent Functional Testing **(3:30)**

Michael Trey Peterson, Christopher Sozio, Bryce Berger, Adam Duncan
NSWC Crane – GXV Trusted & Assured Microelectronics, Crane, IN

Thomas Papish, Grant Skipper
Amentum, Crane, IN

Andrew Lukefahr
Indiana University, Bloomington, IN

10.2: ChipletQuake: On-Die Impedance Sensing for Chiplet and Interposer Verification **(3:50)**

Saleh Khalaj Monfared, Maryam Saadat Safa, Shahin Tajik
Worcester Polytechnic Institute, Worcester, MA

In this article we investigate the usage of impedance analysis to verify the integrity of chiplet-enabled devices in terms of security. We design and implement a fully digital sensor on chiplets and provide hardware level analyzing circuitry for verification purposes. We present ChipletQuake, a hardware design framework to estimate the impedance of the existing chiplets and the interposer on the system. By utilizing arrays of actuators and voltages sensors, we showcase that the estimated impedance of chiplets and interposer can effectively be fingerprinted and any hardware tampering on a neighboring chiplet or the interposer can be detected. We implement our framework on chiplet-enabled FPGA and evaluate it against real-world hardware trojans deployed on chiplets.

10.3: Bitstream Analysis Toolkit **(4:10)**

Bryce Berger, Grant Skipper, Zachary Jordan, Chris Sozio, Adam Duncan
NSWC Crane, Crane, IN

10.4: Combined Trace Neural Network for Improved Design Extraction in Integrated Circuit Post-silicon Verification and Validation Workflows **(4:30)**

Emily Haines, Preston Pozderac, J.Timothy Balint, Yash Patel, Ryan Mattei, James Schaffranek, Adam R. Waite, Adam Kimura
Battelle Memorial Institute, Columbus, OH

Tamara Juntiff, Matt Sale
Air Force Research Laboratory, Wright-Patterson AFB, Dayton, OH

10.5: Post-Silicon Hardware Trojan Detection with High Confidence Leveraging Automated Test Patterns (4:50)

Sudipta Paria, Aritra Dasgupta, Swarup Bhunia
University of Florida, Gainesville, FL

Due to the globalization of the supply chain and the adoption of the zero trust model, hardware Trojans pose significant threats introduced by untrusted entities. Hardware Trojans cause undesired malicious modification in an electronic circuit, resulting in bypassing security measures, altering device functionality, leaking sensitive information, or causing a Denial of Service (DoS) attack. Conventional post-manufacturing testing and test coverage metrics are not sufficient to detect hardware Trojans efficiently without incurring high costs. In this paper, we propose an efficient and scalable test vector generation framework that combines the non-conflicting ATPG-based patterns satisfying the N-detect principle for activating the trigger nets and creating payload-aware virtual Trojans to maximize the likelihood of detecting Trojans while drastically reducing the number of vectors compared to a weighted random pattern-based test generation. We demonstrate that our approach achieves better trigger and Trojan coverage than the state-of-the-art statistical techniques with significantly reduced test length.

DIGITAL II

Tuesday, March 18 / 3:30–5:10 pm / Ballroom H

Chair: **Saverio Fazzari**
Booz Allen Hamilton, Washington, DC

Co-Chair: **Seyi Ayorinde**
Army Research Laboratory, Los Angeles, CA

11.1: Adaptive Radio Frequency System-in-Package – Achieving Spectrum Dominance at the Edge (3:30)

Brian Kimball
Mercury Systems, Inc., Huntsville, AL

Mixed-signal devices have been rapidly advancing in recent years. Analog converter improvements are now enabling Direct RF Sampling and All Digital Sampling, which were previously not possible. Direct RF Sampling allows for digitization of signals directly at RF, rather than having to mix down to (or up from) the IF domain. All Digital Sampling is afforded by the ever-expanding number of transceiver channels provided within a single, SWaP-optimized die. Also, the rise in co-packaged Digital Signal Processing (DSP) affords more efficient pre/post processing of the data prior to downstream/upstream FPGA (Field Programmable Gate Array) ingest/egress. Despite these progressive mixed-signal enhancements, however, end users are still forced to make difficult tradeoffs between bandwidth and dynamic range. Prioritizing bandwidth to collect more data leads to escalating susceptibility to noise and decreased signal quality. Conversely, shifting focus to improved dynamic range leads to a narrower bandwidth, thereby restricting the amount of data.

11.2: MAV-NPU: A 22 nm Sparse Neural Network Processor for Real-Time, Resolution-Scalable Vision of Autonomous Micro Aerial Vehicles (3:50)

Siyuan Chen, Ken Mai
Carnegie Mellon University, Pittsburgh, PA

Real-time environment perception is essential for enabling autonomous navigation of Micro Aerial Vehicles (MAVs). Yet, power and bandwidth constraints limit efficient deployment of NN-based algorithms. MAV-NPU is a sparse neural network processor in 22 nm optimized for MAV vision. It processes a visual odometry network at 52.4 FPS, consuming 27.4 mW and 2.36 MB/frame. MAV-NPU features three key innovations: 1) a model-level Tiled Dataflow adapting to scaling resolution of vision tasks; 2) grouped hierarchical accumulation reducing write-back stalling; 3) an AvgLeakyReLU activation function maintaining hardware utilization. MAV-NPU enables practical deployment of learning-based MAV vision and achieves peak 28.97 TOPs/W.

11.3: Automation of Large-Scale RQL Superconducting Circuits (4:10)

Michael Vesely, Jr., Mehdi Kabir, David Chen
Northrop Grumman Corporation, Linthicum, MD

Anthony Rauhut, Chi Tai, Ian Tomblinson
Cadence Design Systems, San Jose, CA

Recently, superconducting digital circuits have emerged as a promising technology in the post-Moore's law paradigm. Utilizing Josephson junctions as the active switching element, superconducting digital circuits rely on the quantization of magnetic flux (fluxons) to encode binary information. Reciprocal Quantum Logic (RQL) is a leading superconducting logic family that has demonstrated fast, ultralow power operation with wide operating margins. Furthermore, it has shown promising scaling properties producing some of largest, most complex superconducting digital circuits to date. This paper introduces digital design using RQL and explores some of the difficulties encountered during synthesis, timing, and place & routing of RQL circuits. It also describes how these issues have led to novel solutions and features within the Cadence suite of EDA tools to realize digital superconducting circuits. With these advances in EDA tools, RQL technology is poised to achieve magnitude orders of scaling and realize complex superconducting digital circuits.

11.4: A High-Efficiency Dual-Channel Pixel Processor for Event-Based Camera (4:30)

Zhaoqi Wang, Miao He, Yu Feng, Christophe Bobda
University of Florida, Gainesville, FL

Modern sensors' increasing resolution leads to large data volumes and heavy communication loads between imagers and back-end processors, whether in embedded systems or the cloud. Event cameras address this problem by reducing the amount of image data, easing communication strain. However, they require the back-end processor to reconstruct the original image. We introduce an advanced event camera system that incorporates inference directly within the sensor, using an event-based approach to identify important pixels for knowledge extraction. Our pixel processing unit employs a dual-channel filter to capture key pixels from both current and previous frames. In comparison to HARP, the FPGA implementation of our architecture greatly improves computational efficiency and hardware usage, reducing LUT utilization by 94.55%, Flip-Flop usage by 99.39%, and BRAM usage by 29.63%.

11.5: Photonic Fabric Attached Memory for Performance Enhancement in AI Workloads (4:50)

Trung Diep, Jing Ding, Uday Poorsala, Ravi Mahatme
Celestial AI, Santa Clara, CA

Package Input/output (I/O) is a critical parameter for Artificial Intelligence (AI) application specific integrated circuits (ASICs). Conventionally electrical I/O has only been located along two edges of ASICs. This not only caps the maximum off-chip bandwidth but also drives fundamental architectures for ASICs and systems. Celestial AI Photonic Fabric is a revolutionary optical interconnect technology that uses thermally stable optical modulators that can be directly packaged with advanced, high Thermal Design Power (TDP) ASICs. By bypassing the ASIC beachfront, Photonic Fabric can not only deliver >650 Tbps of package bandwidth, but also deliver data directly to the point of consumption within the ASIC. The result is not only new ASIC architectures, but also package and system architecture innovation including a rack mountable Photonic Fabric Appliance. This presentation dives deep into the exciting hyperscale possibilities enabled by the Photonic Fabric for Accelerated Computing.

SWIR AND MWIR IMAGERS

Tuesday, March 18 / 3:30–5:10 pm / Ballroom G

Chair: **Gerald DeJean**
RTX Corporation, Atlanta, GA

Co-Chair: **Steven Palmer**
NIST, Gaithersburg, MD

12.1: An Event-Based MWIR ROIC Operating at High Throughput and Low Contrast Sensitivity **(3:30)**

Roman Fragasse, Megan Manifold, Ramy Tantawy, Shane Smith, Grayson Holloway, Phillip Barker, Nicholas Wells, Gary Sung
SenseICs Corporation, Columbus, OH

Suat Ay
Worcester Polytechnic Institute, Worcester, MA

Waleed Khalil
The Ohio State University, Columbus, OH

12.2: Colloidal Quantum Dot IR Imagers **(3:55)**

Yunrui Jiang, Shaurya Arya, Hexuan Peng, Yu-Hwa Lo
University of California, San Diego, La Jolla, CA

Alan Davis
Naval Undersea Warfare Center (NUWC), Newport, RI

Colloidal quantum dots (CQDs) are revolutionizing the field of infrared imagers at NIR, SWIR and MIR spectra. However, high-performance QD IR detectors have thus far been limited to large-area (millimeter-sized) devices because spin-coated quantum dots are susceptible to performance degradation and reliability issues during the conventional microfabrication processes involving lithography, etching, deposition, etc. Moreover, there is no proper device model for QD detectors and the empirical model from conventional PIN photodiodes performs inadequately for QD detectors. In this paper we present three original contributions we made to advance QD IR imagers: (a) establishing the QD detector model based on device physics, (b) an architectural design to operate IR detection in a photovoltaic mode instead of a photocurrent or charge accumulation mode to overcome the dark current limitations, and (c) development of a unique technology to surmount the challenge of creating pixelated QD structures akin to a conventional CMOS imager.

12.3: High-performance Electrically Reconfigurable NIR-SWIR Metasurface Filters **(4:20)**

Jeong Moon, Kay Son, Ryan Quarfoth, Aaron Bluestone, Hanseung Lee
HRL Laboratories, Malibu, CA

12.4: High Intra-Scene Dynamic Range ROICs Providing Background Suppressed MWIR Imaging **(4:45)**

Roman Fragasse, Megan Manifold, Ramy Tantawy, Shane Smith, Josh Coffey, Ethan Garrett, Nicholas Wells, Gary Sung
SenseICs Corporation, Columbus, OH

Suat Ay
Worcester Polytechnic Institute, Worcester, MA

Waleed Khalil
The Ohio State University, Columbus, OH

WEDNESDAY, MARCH 19

Breakfast, Ballroom Foyer **(7:30–8:30)**

Session 13 **(TA2 – Emerging Technologies)**

NEXT GENERATION MICROELECTRONICS

Wednesday, March 19 / 8:20–10:00 am / Ballroom A

Chair: **Mona Massuda**
Department of Defense

Co-Chair: **Marcia Sawhney**
Department of Defense

13.1: Diamagnetically Levitated and Trapped Graphite Composite Mechanical Resonators (8:20)

Yunong Wang, Alexander Gage, Philip X.-L. Feng
University of Florida, Gainesville, FL

Pooja Roy, Samira Yasmin, Jaesung Lee
University of Central Florida, Orlando, FL

We combine theoretical analyses with experimental investigations to explore the complete diamagnetic levitation of millimeter- to centimeter-scale graphite plates and their rigid body resonances. Leveraging the strong diamagnetic susceptibility of graphite, we employ square graphite plates, which exhibit stable levitation above permanent magnets without requiring active control. The resonance motions of the levitated graphite devices are excited by electrostatic or dielectric gradient forces and detected by using an ultrasensitive optical interferometry system. We observe rigid body resonance modes within a frequency range of f = 25 Hz to 50 Hz with quality (Q) factors of Q = 30–70 at room temperature. Notably, we find that the Q factors are primarily compromised by air damping or eddy current damping. This study represents an initial step toward the development of stabilized levitating systems at room temperature with a large mass. Furthermore, the findings presented here shall contribute to building high-performance future resonant sensors.

13.2: Adiabatic Charge Sharing within Clock Networks in 3-D Voltage Stacked Circuits (8:40)

Andres Ayes, Eby G. Friedman
University of Rochester, Rochester, NY

Adiabatic charge sharing between multiple clock networks within 3-D voltage stacked systems is proposed to save significant power while lowering noise. The technique exploits the proximity of the clock networks to enable mutual charging and discharging when the clock signals transition to the same voltage. During this transition, the clock distribution networks are isolated from the power grid, reducing simultaneous switching noise and current load. The maximum current pulled by the clock network is reduced by approximately 46% as compared to a traditional clocking scheme. The maximum voltage noise is reduced by up to 72% when the clock networks are isolated from the power grids, while the clock networks pull nearly 50% less charge from the source.

13.3: Additively Manufactured Micro-Coaxial Interconnects for Millimeter-Wave Applications (9:00)

Yash Sahoo, Ian Armstrong, Caprice Gray Haley
BAE Systems Inc., Merrimack, NH

Genaro Stoto-Valle, Manos Tentzeris
Georgia Institute of Technology, Atlanta, GA

13.4: Development of Northrop Grumman's N-Polar GaN Technology for Applications at W-band and Beyond **(9:20)**

Jansen Uyeda, Robert Coffie, Sumiko Poust, Hui Ma, Yuguang Hong, Claire Pettiette-Hall, Peter Nam, Sean Armster, Derek King, Ryan Cullen, Floyd Oshita, Sachi Hillard, Ioulia Smorchkova, Reidly Yogi, Matthew Laurent, Ben Heying, Aaron Oki
Northrop Grumman Corporation, Redondo Beach, CA

13.5: MoViD: Physics-Inspired Motion Detection for Satellite Image Analytics and Communication **(9:40)**

Callen MacPhee, Bahram Jalai
University of California, Los Angeles, Los Angeles, CA

Motion detection and analysis are critical tasks in satellite remote sensing, with applications spanning environmental monitoring, urban development tracking, and efficient data storage. In the realm of satellite data processing, change detection and data compression are particularly important challenges that can benefit from advanced motion analysis techniques. This work introduces MoViD (Motion estimation via Virtual dispersion and phase Detection), a novel physics-inspired algorithm that offers a unique perspective on motion analysis grounded in the fundamental physics of temporal group velocity dispersion and phase detection. By virtualizing these phenomena and mapping them to the digital domain, MoViD interprets video data as a spatiotemporal lightfield, harnessing a qualitatively new representation termed spectral phase kinematics. The application of MoViD to satellite data analysis, providing pixelwise motion detection at scale, promises to enhance change detection and data compression capabilities by providing a more nuanced understanding of motion patterns in remote sensor data.

BREAK **(10:00–10:30)**

PACKAGING ECOSYSTEM: ROADMAPS AND FUTURE DIRECTIONS

Wednesday, March 19 / 8:20–10:00 am / Ballroom B

Chair: **Jeremy Rodgers**
Department of Defense

Co-Chair: **Wes Hansford**
Boeing, Huntington Beach, CA

14.1: Adoption of Commercial Advanced Packaging Technologies for Department of Defense Priorities **(8:20)**

Austin Thomas, Fernando Roa
Booz Allen Hamilton, McLean, VA

Justin Borski
TAP Engineering, Columbia, MD

14.2: Noteworthy Semiconductor Advanced Packaging Trends with Government Electronics Implications: 2024–2025 **(8:40)**

Ted Tessier
IBM Semiconductors, Gilbert, AZ

Scott Sikorski
IBM-Semiconductor, Yorktown Heights, NY

14.3: PCB Manufacturing Ecosystem: Opportunities and Challenges **(9:00)**

Antika Roy, Tom Rice-Bladykas, Nitin Varshney, Patrick Craig, Himanandhan Reddy Kottur, Navid Asadizanjani
University of Florida, Gainesville, FL

Pauline Paki
DHS Science and Technology Directorate, Department of Homeland Security, Washington, DC

Printed Circuit Boards (PCBs) are an essential part of modern electronic devices across various sectors, such as consumer electronics, automotive, aerospace, healthcare, and telecommunications. In light of the pandemic as well as global demand and geopolitical issues, countries are striving to establish self-sufficient PCB supply chains within their borders. To address the increasing demand for PCBs and ensure a reliable supply chain, significant efforts are being made to facilitate PCB manufacturing facilities within the United States (US). The US has also enacted the CHIPS and Science Act, which allocates significant funding for semiconductor research and manufacturing incentives to bolster the economy, national security, and supply chain resilience. This study identifies potential bottlenecks in the US PCB supply chain, examines the contributions of US-based companies, and explores their role in the broader economic and technological landscape, aiming to provide insights into current and future PCB manufacturing opportunities in the US.

14.4: Advanced Packaging Design and Manufacturing Flow for Adoption of the On-Shored Chiplet Ecosystem **(9:20)**

Andrew Raseley, Russel Foster, John Allgair
BRIDG – Bridging the Innovation Development Gap, NeoCity, FL

Kurt Sakamoto
KBR Inc., Beavercreek, OH

Priya Kongara, Barry Nelson, David Schwan
Cadence Design Systems, Cary, NC

Daron DiSabato, Luke Duncan
Niobium Microsystems, Columbus, OH

Steve Dooley, Jamin McCue
Air Force Research Laboratory, WPAFB, OH

14.5: A Composable Systems Framework **(9:40)**

Shawn Fetterolf, Joshua Fryman, Christopher George, Tom Rucker
Intel Corporation, Burlington, VT

To accelerate innovation, product development cycles, and reduce development time and cost a new approach to semiconductor architecture is needed. The authors propose a comprehensive standards-based approach to help address these needs through a Composable Systems Framework.

BREAK **(10:00–10:30)**

TRANSITION OF COMPOUND SEMICONDUCTOR TECHNOLOGY AND PHOTONICS

Wednesday, March 19 / 8:20–10:00 am / Ballroom C

Chair: **Vincent Williamson**
Naval Surface Warfare Center – Crane Division, Crane, IN

Co-Chair: **Dmitry Kozak**
Naval Surface Warfare Center – Crane Division, Crane, IN

15.1: T&AM RF/OE Transition Strategy and Engagement **(8:20)**

Joshua Hawke, Vince Williamson, Dmitry Kozak
NSWC Crane, Crane, IN

15.2: Mission Enablement Using the Agilex (TM) 9 SoC FPGA Direct-RF Series with Photonic Data Offload **(8:45)**

Patrick Kenworthy, Marc Angelucci, Greg Fonder
Lockheed Martin, Moorestown, NJ

Jon Wagner
Lockheed Martin, Owego, NY

John Oh, Samson Tam
Altera, an Intel Company, San Jose, CA

15.3: High-Voltage SiC Technology Transitions: Progress and Opportunities **(9:10)**

Miguel Hinojosa, Aivars Lelis
DEVCOM U.S. Army Research Laboratory, Adelphi, MD

15.4: Resilient High-Performance O-RAN Netcentric Equipment (RHONE) **(9:35)**

Jeffrey M. Yang, Matthew T. McNicholas
Northrop Grumman, Redondo Beach, CA

Jenifer S. Foroglou
Northrop Grumman, Melbourne, FL

Michelle K. Treadway
Office of Naval Research Global, Fallon, NV

BREAK **(10:00–10:30)**

DESIGN OF SECURE SYSTEMS

Wednesday, March 19 / 8:20–10:00 am / Ballroom D&E

Chair: **Adam Kimura**
Battelle Memorial Institute, Columbus, OH

Co-Chair: **Jonathan Heiner**
Air Force Materiel Command, Wright-Patterson AFB, OH

16:1: Design, Packaging, Test, and Qualification for SoC-based Obsolescence Mitigation (8:20)

Jeff Durrum, Frank Fradette
Booz Allen Hamilton, Beavercreek, OH

Matt Bergeron
Integra Technologies, Milpitas, CA

Vipul J. Patel, Jamin J. McCue
Air Force Research Laboratory, WPAFB, OH

16.2: MCSE: A Low-Cost Security Engine for Protecting Edge Devices Against Supply-Chain Attacks (8:40)

Emmanuel Elias, Tambiara Tabassum, Kshitij Raj, Atri Chatterjee, Swarup Bhunia, Sandip Ray
University of Florida, Gainesville, FL

Microelectronic devices face increasing vulnerabilities due to globalized and untrustworthy supply chains, making them susceptible to attacks like counterfeiting, overproduction, etc. Addressing these threats while accommodating the strict power, area, and speed (PAS) constraints of modern devices is critical. We introduce MCSE (Minimally Configured Security Engine), a novel FSM-based security architecture that integrates a parameterized subsystem and a CAD flow, enabling customizable protection for devices while balancing power, area, and speed constraints. Unlike traditional microcontroller-based solutions, MCSE provides configurable, plug-and-play protection with minimal overhead. Its ability to balance security needs with device constraints makes it a highly adaptable solution for safeguarding system design in resource-constrained environments.

16.3: TRAP: A Transistor-Level Programmable Fabric for Cost-Effective Hardware Redaction (9:00)

Thomas Broadfoot, Yiorgos Makris, Carl Sechen
University of Texas at Dallas, Richardson, TX

We discuss TRAP, a transistor-level programmable fabric designed for the purpose of cost-effective hardware redaction. TRAP introduces a novel paradigm in the design of hybrid ASIC/programmable integrated circuits (ICs) and can be viewed as a dense sea-of-transistors which can be stitched together to compose logic and state-holding elements. Its unique architecture makes it significantly smaller, faster and less power-consuming than the state-of-the-art programmable fabrics, while its transistor-level granularity makes it impervious to intelligent logic-level attacks. TRAP has been demonstrated in a 12 nm FinFET technology node (GF12LP) and the design of hybrid ASIC/TRAP ICs is supported by largely commercial CAD flow.

16.4: Exploring Accelerated Aging Stress for Physical Unclonable Function Self-Corruption **(9:20)**

Eric Hunt-Schroeder
Marvell Technologies, Inc., Burlington, VT

Tian Xia
University of Vermont, Burlington, VT

This work presents a Pre-Amplifier Physical Unclonable Function (Pre-Amp PUF) with self-corruption function designed and manufactured in a 3-nm FinFET technology. This PUF can perform a destructive read operation as an End of Life (EOL) anti-counterfeit measure against recycled and reused electronics. The destructive read utilizes an accelerated aging technique that exploits both Hot Carrier Injection (HCI) and Bias Temperature Instability (BTI) degradations directly at the PUF entropy source bitcell data. The result is a silicon proven ability to irreversibly corrupt the encryption key, invalidating the PUF key and blocking future authentication attempts. By utilizing HCI and BTI aging effects rather than physical damage we demonstrate a PUF that can self-corrupt its own key without being detectable with imaging techniques. Our technique reuses on-chip stable (repeatable) PUF bitcells identifying circuitry and so minimizes the area overhead to support this differentiated feature.

16.5: FPGA Variation in Voltage Monitoring using On-Chip Time-to-Digital Converters **(9:40)**

David Fatheree, Austin Davis, Casey Fendley, Joel Bjornstad, Seth Cohen
Kratos SRE, Inc., Birmingham, AL

BREAK **(10:00–10:30)**

LTLT

Wednesday, March 19 / 8:20–10:00 am / Ballroom H

Chair: **Yogendra Joshi**
DARPA MTO, Arlington, VA

Co-Chair: **Sina Askari**
DARPA, Arlington, VA

17.1: An Analysis of Power and Performance Improvements from Low-Temperature Operation of Processors using PROCEED-LT (8:20)

Zhichao Chen, Ali H. Hassan, Sudhakar Pamarti, Chih-Kong Ken Yang, Puneet Gupta
University of California, Los Angeles, Los Angeles, CA

Operating processors at low temperatures (LT) can substantially reduce power consumption and enhanced performance in circuit operations by reducing the transistor leakage current, increasing carrier mobility, reducing wear out, and reducing interconnect resistance. We develop PROCEED-LT, a pathfinding framework to co-optimize devices and circuits over a wide performance range. Our results demonstrate that circuit operations at cryogenic temperatures (LT, -196 °C) reduce power compared to room temperature (RT, 85 °C) by 15× to over 23.8× depending on target performance. Alternatively, LT can be operated at the same power point for peak performance improvement of 2.4×. These gains are further improved in low-activity circuits as well as when using multi-voltage configurations. We further highlight the need for improvement in V_{th} variation to leverage benefits at cryogenic temperatures. For intermediate temperatures above cryogenic, a comparison of energy efficiency gains is provided showing that LT conditions can offer substantial benefits even considering the increased cooling cost.

17.2: Optimization of 3 nm High Performance Nanosheet Technology for 77 K Operation (8:40)

J. Frougier, R. Bao, S. Kumar, A. Cestero, R. Joshi, S. Lucarini, A. Chou, S. Emans, S. Siddiqui, H. Trombley, R. Pujari, R. Bonam, R. Robertazzi, C. Baks, C. Waskiewicz, P. Song, L. Qin, E. Miller, E. Leobandung
IBM Semiconductor, Albany, NY

We provided process/integration solutions for high performance Nanosheet technology at 77 K and evaluated its performance benefits. This is the first demonstration of CMOS Nanosheet integration of dual work function metals (WFMs) and dual dipoles at 77 K. WFM engineering plus dual dipole engineering provides target threshold voltage (Vt) solution for Nanosheet technology at 77 K. Nanosheet with low V_{DD} (0.3–0.4 V) at 77 K provides comparable performance to that at 300 K with V_{DD} = 0.75 V, but at much lower power. Nanosheet at 77 K also offers more than 100% performance gain than at 300 K with same V_{DD} = 0.75 V. Junction/contact optimization and multiple Vts (multi-Vt) feasibility were demonstrated. TCAD was also developed to evaluate device performance and variations at 77 K.

17.3: Cryogenic Logic: CMOS Versus Dynamic (9:00)

Ali H. Hassan, Puneet Gupta, Sudhakar Pamarti, Chih-Kong Ken Yang
University of California, Los Angeles, Los Angeles, CA

With adjustments of the threshold voltage of a nanometer-scale device technology and correspondingly the supply voltage, operating processing elements at lowered temperatures such as 77 K can substantially reduce overall energy consumption. Advanced circuit techniques can leverage this reduced-temperature technology for further energy savings. This paper presents a low-temperature, low-Vth (LTLVT) model of a 14-nm FinFET device, calibrated for 77K. By the choice of the threshold and supply voltages, a dynamic-based logic family is shown to further improve energy savings as compared to static CMOS by 40% to achieve 20× energy-delay optimization at 77 K compared to 330 K.

17.4: Design and Optimization of On-Chip Interconnects for Cryogenic Operation (9:20)

Ali H. Hassan, Nathan Lang, Puneet Gupta, Sudhakar Pamarti, Chih-Kong Ken Yang
University of California, Los Angeles, Los Angeles, CA

Digital processing implemented in a technology optimized for reduced temperatures such as 77 K has been shown to significantly improve power dissipation. Operating at cryogenic temperatures benefits active devices but also the properties of passive elements such as interconnects. With well over 30% of gate delay and power dependent on interconnect, this paper focusses on optimizing on-chip metal interconnects based on a technology optimized for cryogenic environments. By refining the metal stack architecture, we achieve substantial improvements, yielding over power savings of 15% for synthesized logic and over 30% for buffers at 77 K. The results are validated in a 16-nm-class FinFET technology.

17.5: A 10 GHz Low-Power and Low-Jitter PLL for Resonant Clock Forwarding in Wireline Transceivers Operating at Cryogenic Temperatures (9:40)

Mohammadreza Zeinali, Chih-Kong Ken Yang, Sudhakar Pamarti
University of California, Los Angeles, Los Angeles, CA

BREAK (10:00–10:30)

SPCE

Wednesday, March 19 / 8:20–10:00 am / Ballroom G

Chair: **Todd Bauer**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Pierre Auroux**
Technical Consultant, Rockville, MD

18.1: Establishing Capabilities for GaN Enabled Heterogenous 48 V to 1 V Power Conversion Supporting Applications with a Radiation Environment **(8:20)**

Thomas E. Byrd, Antuwon H. Butler
Lockheed Martin MFC, Grand Prairie, TX

Michael J. Podel
Lockheed Martin MFC, Orlando, FL

Robert P. Strittmatter
Efficient Power Conversion, El Segundo, CA

Aarranon Bharathan, Dragan Maksimovic
University of Colorado, Boulder, Boulder, CO

Rabindra Das
MIT Lincoln Labs, Lexington, MA

18.2: Toward Radiation Tolerant Point-of-Load Conversion in SLCFET Transistors **(8:40)**

Benjamin Grisafe, Timothy Vasen, Kenneth J. Myers, Scott K. Suko, Kevin Galiano, Lyndsey Rotella, Robert S. Howell, Patrick Shea
Northrop Grumman Mission Systems, Linthicum Heights, MD

18.3: Radiation-Tolerant Point of Load Converter (R-POLC) **(9:00)**

Vivek Mehrotra, Keisuke Shinohara, Dean Regan, Logan Whitaker, Joel Wong, Philip Stupar, Emil Hanna
Teledyne Scientific & Imaging, Thousand Oaks, CA

Rongming Chu
Pennsylvania State University, University Park, PA

Jian Sun
Rensselaer Polytechnic Institute, Troy, NY

Under DARPA SPCE program, we are developing a dc-dc converter for direct conversion of 48 V input to <1 V output. We are developing solutions for: (i) direct conversion without an intermediary bus voltage, (ii) inherently increasing the radiation tolerance of E-mode GaN devices, (iii) increasing switching frequency to reduce size of passives while keeping efficiency high, (iv) reducing the simultaneous voltage, current and ionizing radiation stresses to prevent single event burnouts, and (v) integration techniques that reduce parasitics and ohmic losses in the interconnects. We will present a 4-cell series capacitor-buck (SC-buck) circuit that solves the problem of extremely short on-time of high side switch in conventional buck converter. The 4-cell SC-buck utilizes normally off super-heterojunction GaN switches with >3× higher breakdown field due to uniform electric field compared to existing GaN devices, and microfabricated inductors with magnetic core and interconnect terminations for direct bonding, thereby enabling 2.5D and 3D integration.

18.4: Rad Hard GaN HEMT Based Ultra-High Density 48 V-to-PoL Converter **(9:20)**

Eric Faraci, Srinivasan Kannan
IR HiRel, an Infineon Technologies Company, Andover, MA

Nathan Ellis, Robert Pilawa-Podgurski
Power Integration Laboratory, LLC, Alamedia, CA

Leora Peltz, Karim Boutros, Jose Garcia
The Boeing Company, Huntington Beach, CA

A new 100 V radiation hardened power GaN HEMT is introduced. This device has been modified from commercial Infineon GaN to improve performance against heavy ion strikes, with discussion on parametric and catastrophic failure mechanisms and how impact was mitigated. Results include measured SEE test results. Additionally technology maturation, with focus on unique aspects of GaN like dynamic $R_{DS(on)}$ and how to properly determine failure rate which includes impact from very low defect densities, are discussed. System level benefits that this GaN enables are shown with it used in a novel switched capacitor-based series capacitor buck topology in a 50 W 48 V-to-PoL converter. Improvements over existing solutions is further extended by combining performance improvement of GaN and topology innovations that reduce size of passive components to enable best in class efficiency and power density exceeding 2 kW/in^3. Results include measured COTS prototype hardware results and space grade prototype simulation results.

18.5: 3D Heterogeneously-Integrated Miniaturized Point-of-Load Converter for Space with Onshore Low Q_g*R_{on} E-mode GaN and Multi-MHz Control ASIC **(9:40)**

Steve Lapen, Mike Wojtowicz, Tim Hsia, Joe Nedy, Rob Coffie, Wen-Ben Luo, Chris Grossman, Jessica Sui, Nancy Lin, Andrew Carter, Yuguang Hong, Floyd Oshita, Aaron Oki, Josh O'Malley, Sean Hamilton, Sam Saunders, Victor Lee, Bob Weebe
Northrop Grumman Space Systems, Redondo Beach, CA

Ian Winfield, Mike Matthews, Nichole Miller
Fabric8Labs, San Diego, CA

Modern digital processors and RF electronics continue to advance into ever smaller packages, while requiring high current/low voltage point-of-load power. The DC-DC converters powering them have become a limiting factor for overall system size and efficiency. This problem is particularly acute for space systems, where the radiation and vacuum environment pose additional constraints on miniaturization. This paper meets the challenge with 3D heterogeneous integration (3DHI) technology, advanced GaN switching transistors, additive-manufactured copper, and control circuits that enable multi-MHz switching frequency to minimize volume of power filter components. Prototype test results from onshore, high-performance e-mode GaN switching HEMTs grown on a SiC substrate and targeting use in a space radiation environment are discussed. The work includes a power converter control ASIC supporting switching frequencies up to 10 MHz. These technologies will be integrated in a 48:1 V / 50 A output point-of-load power converter under the DARPA SPCE (Space Power Conversion Electronics) program.

BREAK **(10:00–10:30)**

PHOTONIC INTEGRATED CIRCUITS AT VISIBLE WAVELENGTHS

Wednesday, March 19 / 8:20–9:35 am / Ballroom F

Chair: **Nicholas Usechak**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Jim Adleman**
SPAWAR, San Diego, CA

19.1: Quantum Integrated Photonics Foundry-scale Platform **(8:20)**

Michael Fanto
USAF/AFRL/RITQ, Rome, NY

Gerald Leake
AIM Photonics, Albany, NY

19.2: Photonic Integrated Circuits for Rubidium-Based Quantum Sensors **(8:45)**

Chong Zhang, Minh Tran, Tin Komljenovic
Nexus Photonics, Goleta, CA

19.4: Short Wavelength Photonic Platform for RF Photonic Processing **(9:10)**

Michael Gehl, Scott Madaras, Nicholas Boynton, Thomas Friedmann, Matthew Boady, Andrew Starbuck
Sandia National Laboratories, Albuquerque, NM

Douglas Trotter
Douglas Trotter Consulting, LLC, Albuquerque, NM

BREAK **(10:00–10:30)**

QUANTUM ARCHITECTURE AND DESIGN

Wednesday, March 19 / 10:30 am–12:10 pm / Ballroom A

Chair: **Michael Lovellette**
The Aerospace Corporation, Chantilly, VA

Co-Chair: **Jeremy Muldavin**
SecureFoundry, Annandale, VA

20.1: Efficient Quantum Circuit Design with a Standard Cell Approach (10:30)

Evan E. Dobbs, Alexandru Paler
Aalto University, Espoo, Finland

Joseph S. Friedman
University of Texas at Dallas, Richardson, TX

We propose the design of quantum circuits by using the standard cell approach borrowed from classical circuit design, which can speed up the layout of circuits with a regular structure. Our standard cells are general and can be used for all types of quantum circuits: error-corrected or not. We use cubic standard cells for Toffoli gates and, starting from a 3D architecture, we design a multiplication circuit. We present evidence that, when compared with automatic routing methods, our layout-aware routers are significantly faster and achieve shallower 3D circuits (by at least 2.5×), while also reducing routing costs. Additionally, our co-design approach can be used to estimate the resources necessary for a quantum computation without using complex compilation methods. We conclude that standard cells, with the support of layout-aware routing, pave the way to very large scale methods for quantum circuit compilation.

20.2: Magnetic Field-Mediated Superconducting Logic (10:55)

Alexander J. Edwards
University of Texas at Dallas, Richardson, TX
and
Laboratory for Physical Sciences, College Park, MD

Son T. Le, Jeffrey Schwartz, Nicholas A. Blumenschein, Aubrey T. Hanbicki, Adam L. Friedman
Laboratory for Physical Sciences, College Park, MD

Ebenezer C. Usih, Joseph S. Friedman
University of Texas at Dallas, Richardson, TX

While superconductors are highly attractive for energy-efficient computing, fundamental limitations in the logic styles have hindered scaling and increased energy consumption. We therefore propose and experimentally demonstrate a novel superconducting switching device utilizing the stray magnetic field from a spin-orbit torque-switched magnet to control the resistivity of a superconductor. We further propose a complete logic family comprised solely of these devices that has the potential to drastically outperform extant superconducting logic families in terms of energy efficiency and scalability.

20.3: Scalable Error Detection and Verification for Enhanced Quantum Computing (11:20)

Navnil Choudhury, Kanad Basu
University of Texas at Dallas, Richardson, TX

Quantum circuit transpilation significantly alters input circuits by decomposing complex operations into hardware-compatible gates, thereby requiring rigorous verification to ensure correctness. In this paper, we present a comprehensive verification framework that addresses the challenges posed by quantum circuit transpilation. This framework integrates QuBEC, a Binary Decision Diagram (BDD)-based approach for equivalence checking, augmented with quantum error correction (QEC) mechanisms. While BDD-based formal verification offers exhaustive coverage of all circuit states and operations, we complement this with simulation-based verification to overcome the resource-intensive nature of formal methods for large-scale circuits. When evaluated on state-of-the-art benchmark circuits, both approaches demonstrate high verification accuracy, exhibiting their efficacy.

20.4: Partitioning SFQ Circuits for Current Recycling with Driver-Receiver Pair Insertion (11:45)

Tejumadejesu Oluwadamilare, Eby G. Friedman
University of Rochester, Rochester, NY

A significant challenge in single flux quantum (SFQ) technology is the large current requirement, which can lead to failure at currents exceeding two amperes. To address this issue, serial biasing of SFQ circuits has been proposed. In serial biasing, similar circuits are divided into several blocks, with each block placed on a different ground plane. However, due to the isolated ground planes, a driver-receiver pair is necessary to transfer signals between blocks on the isolated ground planes. To reduce the bias current requirements while minimizing the number of signals exchanged between adjacent blocks, a partitioning technique for heterogeneous circuits is proposed. This heterogeneous partitioning is demonstrated on ISCAS'89 benchmark circuits, employing resistive trees and heterogeneous current recycling techniques. The partitioned circuits exhibit an average bias current reduction of 54% with a Josephson junction overhead of 3.6%.

LUNCH (12:10–1:30)

CHIPLETS: TECHNOLOGIES AND STANDARDS

Wednesday, March 19 / 10:30–11:50 am / Ballroom B

Chair: **Robert Harris**
Georgia Tech Research Institute, Atlanta, GA

Co-Chair: **Robert Freeman**
Synopsys, Inc., Sunnyvale, CA

21.1: Raytheon-Made Silicon Interposers for UCIe (10:30)

Matthew Tyhach, Aaron George, Sean Kilcoyne, Eric Miller, Jason Milne
Raytheon, Tewksbury, MA, El Segundo, CA, San Diego, CA and Lompoc, CA

21.2: Toward a Self-Organizing Plug and Play Chiplet Architecture and Standard (10:50)

John DeVale, Ryan Rakvic
Intel Corporation, Washington, DC

Keith Lynn
Lockheed Martin Corporation, Boston, MA

The design and manufacturing of System-on-Chip (SoC) technology at advanced nodes is costly, especially for organizations with lower production volumes. This often leads to mission-critical systems using outdated nodes that can no longer deliver optimal performance. Chiplets offer a modern solution yet still create integration challenges, even with standard interconnects like UCIE and AIB. The Department of Defense (DoD) requires a simplified approach to chiplet integration, similar in ease to adding expansion cards to a motherboard. In this work, we propose introducing higher-level standards to manage the complexity of integration. Using standard chiplet landing zones, a self-organizing architecture leaves only the selection of mix and match, plug and play chiplets to enable using advanced ASIC process nodes. A successful chiplet architecture would abstract technical complexities, enabling flexibility and cost-efficiency, driving innovation and capability in the DoD mission space and beyond.

21.3: Chiplet Testing to Enable System Solutions through Heterogeneous Integration (11:10)

Salem Abdennadher
Intel, Laguna Beach, CA

Tao Zhou
Intel, San Diego, CA

With the chiplet model gaining momentum as an alternative to developing monolithic SoC designs, testing is becoming one of the major enablers of a wider adoption of chiplet ecosystem. Chiplets and D2D interconnect raises complex test challenges that are driving new standards and DfT approaches to advanced-package testing. In multi-die packages, one defective die can result in the failure of the whole package. Heterogenous integration within the package involve complexities that drive the need for effective inspection for high yields. This paper addresses the test challenges and emerging solutions for testing D2D interconnect and chiplets. This paper will set these all within the context of the current industry test standards regarding workflow and test formats; and concludes with a set of recommendations and suggested next steps. The goal of this paper is to define chiplet testing considerations, challenges, and available solution frameworks to enable efficient testing of heterogenous systems.

21.4: Additive Manufacturing of Passive and Active Components for Chiplets and Heterogenous Integration (11:30)

Ahmed Busnaina, Sudhir Jain
Nano OPS, Inc., Burlington, MA

We introduce a new additive and scalable manufacturing technology for making passive and active electronic components, as well as trace and interconnects at the nano and microscale. The technique eliminates etching, vacuum deposition, and other chemically intensive processing by utilizing direct assembly of nanoscale particles or other nanomaterials onto a substrate precisely where the structures are built. The technology utilizes inorganic materials such as metals, silicon, and II-VI semiconductors and dielectrics such as SiO2, HfO2, and Al2O3. The technology demonstrated the printing of single-crystal conductors and semiconductors. The technology enables making passive and active components at the nano and microscale using a purely additive (directed assembly enabled) process utilizing inorganic semiconductors, metals, and dielectrics nanoparticles suspended using colloid chemistry and post-assembly crystallization using different annealing conditions. The process demonstrates the manufacturing of transistors with an on/off ratio greater than 106.

LUNCH (12:10–1:30)

COFFEE

Wednesday, March 19 / 10:30 am–12:10 pm / Ballroom C

Chair: **Todd Bauer**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Zachary Fishman**
Booz Allen Hamilton, Washington DC

22.1: Understanding Nanoacoustics Scalability for the Manufacturing of K-band RF Front-Ends **(10:30)**

Luca Colombo, Gabriel Giribaldi, Matteo Rinaldi
Northeastern University, Boston, MA

Adam Peczalski, Eduardo M. Chumbes
RTX, Andover, MA

Jeffrey LaRoche
RTX, Tewskbury, MA

22.2: Millimeter-Wave Miniaturized Resonators and Filters in Piezoelectric Thin-Film Lithium Niobate **(10:50)**

Jack Kramer, Omar Barrera, Sinwoo Cho, Vakhtang Chulukhadze, Ian Anderson, Joshua Campbell, Tzu-Hsuan Hsu, Ruochen Lu
University of Texas at Austin, Austin, TX

Lezli Matto, Kenny Huynh, Michael Liao, Mark S. Goorsky
University of California Los Angeles, Los Angeles, CA

The need for compact front end signal processing elements spurred the development of surface and bulk acoustic wave devices for mobile applications. Now, similar needs push to advance these technologies to the millimeter wave. In this work, we demonstrate advances to the established thin film lithium niobate platform to enable acoustic resonators above 100 GHz and filters up to 50 GHz. This platform enables us to achieve state-of-the-art performance in low loss millimeter acoustics.

22.3: Continuously Tunable Magnetostatic Wave Filters Enabled by Miniaturized Electromagnetic Assemblies **(11:10)**

Bill Zivasatienraj, Eric Langlois, Michael Cason, Renyuan Wang
BAE Systems, Inc., Nashua, NH

Sudhanshu Tiwari, Connor Devitt, Sunil Bhave
Purdue University, West Lafayette, IN

22.4: X-Ku Band, High Performance Resonators and Filters Based on Periodically Poled Aluminum Scandium Nitride Films **(11:30)**

Merrilyn Mercy Adzo Fiagbenu, Shun Yao, Yang Deng, Izhar, Xingyu Du, Roy H. Olsson III
University of Pennsylvania, Philadelphia, PA

Craig Moe, Pinal Patel, Mojtaba Hodjat-Shamami, Daeho Kim, Siddhant Sahoo, Ramakrishna Vetury
Akoustis, Inc., Huntersville, NC

22.5: Aluminum Nitride Resonant Pressure Sensors for High Temperature Applications (11:50)

Azadeh Ansari, Seyyed Mojtaba Hassani Gangaraj, Tanya Chauhun
Georgia Tech, Atlanta, GA

Mingyo Park
Penn State University, State College, PA

This work reports on Aluminum Nitride (AlN) resonant pressure sensors, fabricated on top of bulk AlN substrate. The transducer is fabricated by transferring sputtered Mo/AlN/Mo stack to a bulk AlN substrate, and allowing for intimate integration of AlN MEMS with AlN electronics. The resonant transducer shows an ultra-high frequency – pressure sensitivity by taking advantage of a thin air cavity, in pressure equilibrium with the ambient. The restoring force applied to the thin oscillating membrane by the trapped gas in the cavity, modulates the membrane stiffness and therefore its resonance frequency. We demonstrate a linear and increasing frequency versus pressure trend that is the highest reported for any AlN resonant pressure sensor to date. Furthermore, we demonstrate high quality factor thickness extensional (TE) resonance modes of the same transducers, measured up to 400 °C, and compared before and after 800 °C annealing for 30 minutes.

LUNCH (12:10–1:30)

Session 23: **(TA10 – Trusted, Assured and Cyber-secure Microelectronics)**

MODELS AND MEASUREMENTS

Wednesday, March 19 / 10:30 am–12:10 pm / Ballroom D&E

Chair: **Samson Melamed**
Code Metal, Inc., Boston, MA

Co-Chair: **Vivian Kammler**
Sandia National Laboratories, Albuquerque, NM

23.1: Development of a Digital Twin for the reFLX Tool: Enabling Virtual Prototyping and Security Feature Integration for Semiconductor Design **(10:30)**

Denis Shamiryan, Jordan Vos, Lex Keen
SecureFoundry, Inc., Fort Worth, TX

Marcus Emanuel, Hongbin Choi, Matthew Maniscalco, Todor Bliznakov, Nicholas May, Toni Moore, Sina Shahbazmohamadi, Pouya Tavousi
University of Connecticut, Storrs, CT

This paper presents the development of a comprehensive digital twin for the reFLX tool, a high-throughput, maskless e-beam direct write system that employs multiple e-beams in parallel to enable rapid semiconductor fabrication. Through the digital twin, users can simulate the fabrication process, virtually test their designs, and iterate changes before committing to physical production. The ability to virtually inspect designs, evaluate process changes, and perform electrical and performance simulations significantly reduces development time and cost. Moreover, the reFLX tool's direct-write capability allows for the embedding of unique security features, which can be investigated and optimized virtually through the platform. These features not only protect intellectual property but also act as anti-counterfeiting measures, making the digital twin a powerful tool for both design optimization and security feature implementation.

23.2: CHASM: Composable System Security Modeling Helping Assurance Solution Measurements **(10:50)**

Christopher Taylor, Eric Bauer, Zach Allen, Lydia Carter, Vince McKinsey, Jacob Haehn, Aaron Ruen
Battelle Memorial Institute, Columbus, OH

Matthew D. Sale
Air Force Research Lab, Dayton, OH

23.3: Physical Model-Assisted Secure Software Execution Against Fault-Injection Attacks **(11:10)**

Henian Li, Md. Habibur Rahman, Arunabho Basu, Rakibul Hassan, Farimah Farahmandi, Mark M. Tehranipoor
University of Florida, Gainesville, FL

Modern software running on vulnerable circuits such as SoCs and processors is increasingly susceptible to cyber and hardware attacks. While protections against cyberattacks are widely integrated across the software development and compilation cycle, physical attacks such as fault-injection attacks directly target hardware implementations. Such attacks bypass upper-level protections and compromise the confidentiality, integrity, and availability of modern chips. Since the hardware has already been fabricated, the cost of redesign is extremely high, hence hardening software/firmware against the identified physical vulnerabilities would be a recommended and less costly approach. However, existing compilers lack considerations and hardening techniques for physical attacks. In this paper, we address physical threats from fault

injections at the software compilation stage. Our approach models fault-injection attacks based on physical design characteristics, facilitating secure software compilations with low-cost and effective physically-aware hardening techniques.

23.4: Measuring the Security of Zero-Trust Architecture-based Systems-on-Chip (11:30)

Abigail Butka, Christophe Bobda
University of Florida, Gainesville, FL

Zero-Trust Architectures (ZTA), proposed by the National Institute of Standards and Technology (NIST), improves security through a strict ‘never trust, always verify’ ideology. Although originally developed for network security, applying ZTA to Systems-on-Chip (SoCs) addresses a critical issue: the integration of third-party components that may be untrustworthy or malicious. This paper proposes a component-level metric and rubric to evaluate SoC adherence to the key principles of ZTA. The metric focuses on assessing the impact, vulnerability, and logging of each component’s registers to identify the most at-risk system components. The rubric assists SoC designers in mitigating identified risks by providing clear guidelines for improving impact, vulnerability, and logging. This method accounts for the unique architecture and integration of hardware and software in SoCs as well as provides designers a clearer understanding of their system’s security posture and a roadmap for aligning SoCs with ZTA principles

23.5: Establishing Evidence-based Assurance for Commercial Third Party Processor IP (11:50)

Jason Oberg, Will Cummings, Jagadish Nayak
Cycuity, Inc., San Jose, CA

Gayatri Perlin, Richard Ferguson, Steve Kim, Seung Moon
BAE Systems, Inc., Burlington, MA

Mark Le, Trevor McKay
SiFive, Inc., Santa Clara, CA

Jamin McCue
Air Force Research Laboratory, WPAFB, OH

This work demonstrates the successful pilot of evidence-based assurance starting with commercial third-party intellectual property (3PIP) through the integration, configuration, and security verification of the 3PIP in a system-on-chip (SoC). We present a methodology using the hardware Common Weakness Enumeration (CWE) to prioritize, create, and verify design-specific security requirements in support of evidence-based assurance. Furthermore, we demonstrate the scalability, deployability, and effectiveness of the solution on a large-scale commercial 3PIP from SiFive, Inc. integrated into a BAE Systems’ radiation hardened SoC intended for future use in DoD programs of record. We discuss the methodology, analyze the results, and provide suggestions for future work.

LUNCH (12:10–1:30)

ANALOG AND MIXED-SIGNAL CIRCUITS

Wednesday, March 19 / 10:30 am–12:10 pm / Ballroom H

Chair: **Saverio Fazzari**
Booz Allen Hamilton, Washington DC

Co-Chair: **Abirami Sivananthan**
InQTel, Arlington, VA

24.1: A DC to 50 GHz High Input Impedance Amplifier Supporting an Ultra-Wide Input Range for Oscilloscope on Probe-Tip Applications (10:30)

Jesse Moody, Patrick Finnegan, Chris Nordquist, Tyler Liebsch
Sandia National Labs, Albuquerque, NM

This work presents an ultra-broadband DC-coupled and high input impedance RF amplifier for oscilloscope on probe-tip applications. This device presents a unique combination of ultra-wide bandwidth, wide input swing (>600 mV pk-pk), and nearly 3.0 V input DC voltage range. The device presents an exceptionally high input impedance (90 fF) without using pole-zero doublet-based attenuation improving input referred noise, while offering near unity gain to over 50 GHz. This bandwidth is achieved through adoption of an ultra-wide bandwidth op-amp based input stage with low loop gain ensuring stability, and a three-way pole splitting network for maximum bandwidth extension. A negative supply voltage along with floating body PD-SOI devices enables the rails of this device to be set depending on the DC voltage level to be observed. When heterogeneously integrated into a microprobe assembly this device offers an excellent solution for debugging dense and ultra-high speed heterogeneously integrated devices.

24.2: System-on-Module Enhancement via Wideband Direct Quadrature-Interleaving (10:50)

W. Michael Jones, Stephen Pancrazio, Bryce Readyhough, Connor Bryant
Analog Devices, Inc., Durham, NC

A compact digitizer in the 3U VPX form factor leverages an RF personality tuner card for direct quadrature sampling. The 2-channel transmit, 2-channel receive module uses a digitizer base-card with a pair of interleaved ADCs sampling at 20 GSPS to create a 40 GSPS effective channel rate. The digitizer base-card ADC and DAC performances are characterized across the frequency band of interest. The RF personality card leverages adjacent ADC inputs to effectively double the bandwidth for a given channel. By virtue of this quadrature-interleaving strategy, the digitizer sample rate is doubled, thereby creating a 20 GHz Nyquist zone that offers Ku-band direct-sampling without a Nyquist boundary.

24.3: Direct RF Sampling Converters and Chiplet in Intel 18A Technology **(11:10)**

Issy Kipnis
Intel Corporation, Santa Clara, CA

Tao Zhou
Intel Corporation, Santa Diego, CA

Direct RF sampling converters directly digitize RF signals; operating the converters at high sampling rates enables dynamic selection of frequency bands, large analog/RF bandwidths and multimode signals. Next generation direct RF sampling converters IP or chiplets need to be implemented on silicon processes that feature best-in-class power/performance/area (PPA) logic as well as competitive analog performance with reduced overall power and area. Intel18A process is uniquely suited to achieve these stringent requirements.

24.4: Energy-Efficient Co-Design for Octave Convolution in Deep Neural Networks Using ReRAM Crossbars **(11:30)**

Abrar Abdurrob, Emre Salman
Stony Brook University (SUNY), Stony Brook, NY

Jack Lombardi
Air Force Research Laboratory, Rome, NY

24.5: Small Area, Highly Linear, Modified Hybrid R-2R-Capacitor Digital-To-Analog Converters with Real Time Digital Calibration Algorithm **(11:50)**

Ekaniyere Oko-Odion, Emmanuel Nti Darko, Isaac Bruce, Matthew Crabb, Degang Chen
Iowa State University, Ames, IA

This paper presents the design of a highly compact modified resistor R-2R capacitor hybrid digital-to-analog converter (DAC) with integrated redundancy. The proposed approach leverages redundancy and topological modifications to enhance linearity while significantly reducing the circuit area. This technique enables the implementation of a compact DAC without the need for stringent component matching. Additionally, we introduce a low-latency, memory-efficient, and computationally efficient calibration algorithm. This algorithm effectively calibrates both negative and large positive output jumps, thereby eliminating the necessity for sub-radix DACs to mitigate positive jumps. The design was validated through simulations in TSMC 180 nm technology, demonstrating post-calibration performance with a 14-bit integral nonlinearity (INL) and differential nonlinearity (DNL) of ±0.5 LSB and ±1 LSB, respectively, despite requiring only a 5-bit matching performance.

LUNCH **(12:10–1:30)**

GaN POWER ELECTRONICS

Wednesday, March 19 / 10:30 am–12:10 pm / Ballroom G

Chair: **Travis Anderson**
University of Florida, Gainesville, FL

Co-Chair: **Michael Mastro**
U.S. Naval Research Laboratory, Washington, DC

25.1: Robust Operation of 3.3 kV Planar GaN Diodes with High Temperature Reverse Bias Stress **(10:30)**

Alan Jacobs, James Lundh, James Gallagher, Karl Hobart, Michael Mastro
US Naval Research Lab, Washington, DC

Travis Anderson
University of Florida, Gainesville, FL

Geoffrey Foster
Jacobs Inc., Residing at NRL, Washington, DC

Brendan Gunning, Robert Kaplar
Sandia National Labs, Albuquerque, NM

25.2: AlGaN/GaN Super-Heterojunction Normally-Off Sidewall Gated MOSFET with Optimized Linear Graded AlGaN Design **(10:50)**

Rian Guan, Jianan Song, Rongming Chu
Pennsylvania State University, University Park, PA

Andy Xie
Qorvo, Richardson, TX

By deploying the Super-heterojunction (SHJ) technique, AlGaN/GaN MOSFETs have been demonstrated experimentally with 10 kV blocking voltage and mitigated current collapse switching at 3 kV. However, the threshold voltage of the previously reported AlGaN/GaN SHJ MOSFET was around 0 V, which complicates the gate driver design. To resolve this issue, we propose a new device structure by forming gate structure on the sidewall of the p-GaN, pushing the threshold voltage to above 0 V to achieve normally-off characteristics. This design also promises a higher tolerance to heavy ion single-event effects. This paper describes the concept of this new device structure and our recent progress in implementing this structure.

25.3: Experimental Measurement of Impact Ionization Coefficients in High-Al Content AlGaN **(11:10)**

Z. Zhu, L. Cao, J. Xiong, M. Gutierrez, Y. Duan, W. Turner, A. J. Hoffman, and P. Fay
University of Notre Dame, Notre Dame, IN

Y. Satapathay, S. Pavlidis, R. Collazo, Z. Sitar
North Carolina State University, Raleigh, NC

P. Reddy, R. Kirste, S. Mita, W. Mecouch, Z. Sitar
Adroit Materials, Cary, NC

Ultra-wide band gap semiconductors such as high-Al-content $Al_xGa_{1-x}N$ are attractive materials for devices in both power switching and high-power RF applications. Detailed knowledge of the impact ionization coefficients is essential for the design of RF and power transistors, as well as devices such as IMPATT diodes and avalanche photodiodes (APDs) that rely explicitly on avalanche phenomena. While numerical predictions of the impact ionization

coefficients of high-Al content $Al_xGa_{1-x}N$ have been reported previously, to date no reports of measured or experimentally-extracted impact ionization coefficients are available. We present the first experimental characterization of the electron impact ionization coefficients for $Al_xGa_{1-x}N$ with 60%–65% Al content.

25.4: Single Event Radiation Impact on Various GaN Devices **(11:30)**

Mona Ebrish, Aditha Senarath, Swarnim Neema, Owen Meilander, Dennis Ball, Josh Caldwell, Daniel Fleetwood, Ronald Schrimpf
Vanderbilt University, Nashville, TN

Alan Jacobs
Naval Research Laboratory, Washington, DC

Travis Anderson
University of Florida, Gainesville, FL

Robert Kaplar
Sandia National Laboratory, Albuquerque, NM

The breakdown voltage derating due to radiation effects is the biggest challenge for GaN power devices in harsh environments and space applications. The derating takes away from their higher critical electric field advantage. In this work we investigated two different GaN based devices from the lens of single event burnout (SEB). Our work quantifies the role of electric field management, and the substrate properties. We observed that edge termination design has a significant impact on the de-rating factor of diodes while in transistors the buffer layer just below the channel region is crucial in governing the sub-channel leakage path

25.5: kV-Class Vertical GaN Junction Barrier Schottky (JBS) Diodes via Doping and Contact Engineering **(11:50)**

Matt Alessi, Md Azizul Hasan, Shane Stein, Spyridon Pavlidis, Shashwat Rathknathiwar, Erhard Kohn, Zlatko Sitar, Ramón Collazo
NC State University, Raleigh, NC

Dolar Khachariya, William Mecouch, Seiji Mita, Pramod Reddy, James Tweedie, Ronny Kirste, Zlatko Sitar
Adroit Materials, Cary, NC

Kacper Sierakowski, Grzegorz Kamler, Michal Bockowski
Institute of High Pressure Physics of the Polish Academy of Sciences, Warsaw, Poland

Vertical GaN power devices can reduce the losses and size of power conversion systems used in both commercial and defense platforms. Recently, effective activation of implanted Mg in homoepitaxial GaN has been demonstrated via ultra-high pressure annealing (UHPA), leading to reports of vertical GaN junction barrier Schottky (JBS) diodes with promising performance. Here, we analyze the performance of GaN JBS with up to 1.9 kV breakdown voltage and a corresponding Baliga Figure of Merit (BFOM) of 1.9 $GW \cdot cm^{-2}$. Via modeling and test structure analysis, it is demonstrated that significant Mg diffusion lowers surface concentration and produces graded junctions. In response, we investigate layout trade-offs to offset the impact of Mg redistribution due to UHPA, and propose the use of evaporated Mg in ohmic contacts to p-GaN with reduced surface concentrations. These results inform next-generation vertical GaN power device design and manufacturing.

LUNCH **(12:10–1:30)**

PHOTONICS APPLICATIONS

Wednesday, March 19 / 10:30–11:45 am / Ballroom F

Chair: **Paul Devgan**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Nicholas Usechak**
Air Force Research Laboratory, Wright-Patterson AFB, OH

26.1: Chip-Scale Photonic True-Time Delay Beamformer for RF Phased Array Antenna (10:30)

Stephen R. Anderson, Weimin Zhou
DEVCOM ARL Army Research Directorate, Adelphi, MD

The RF-Photonic platform promises to deliver true time delay beamforming in a low size and weight form-factor, providing wideband, frequency-agile performance in a chip-scale package. Selected architectures for a cascaded 30-element RF-photonic beamformer are designed and fabricated through the AIM Photonics foundry. Thermally tunable ring-resonators switch RF-modulated C-band light into differing path-lengths, creating true-time delay between adjacent beamformer outputs. The cascaded architecture relaxes the total required delay supplied by the individual true time delay units.

26.2: Space and Energy Efficient Satellite Communication Link Enabled by Stepped Quantum Well Modulators (10:55)

Nathaniel Coirier, Hooman Mohseni
Northwestern University, Evanston, IL

An intersatellite communication link using retroreflecting stepped quantum well modulators is proposed. Extrapolating link performance from experimental measurements of stepped quantum well modulators suggests improved system bandwidth, size/weight, and power consumption when compared to existing RF and optical communication links.

26.3: Radiation-Hardened Silicon Photonic Integrated Circuits for Space Applications (11:20)

Kevin Mienta, Biswajit Ray, Mahdi Nikdast
Colorado State University, Fort Collins, CO

There has been growing interest in utilizing silicon photonic integrated circuits (PICs) for both near-Earth and deep space communication applications. This interest is driven by the need to meet the surging demands for terabit optical communication, with expected downlink capabilities increasing tenfold over the next decade, while also achieving substantial improvements in size, weight, power, and cost (SWaP). However, given the intense radiation in space environments, it is essential to assess how space radiation affects the photonic and electronic components within PICs. In this paper, we review some opportunities and challenges to realize radiation-hardened PICs for space applications while reporting our work in this area.

LUNCH **(12:10–1:30)**

QUANTUM MEASUREMENT AND APPLICATIONS

Wednesday, March 19 / 1:30–3:10 pm / Ballroom A

Chair: **La Vida Cooper**
NASA Goddard Space Flight Center, Greenbelt, MD

Co-Chair: **Michael Lovellette**
The Aerospace Corporation, Chantilly, VA

27.1: All-Fiber-Connected Telecom Entangled Photon Source (1:30)

Wei Zung Chang, Ethan H. Tucker, Andrew K. Mollner, Carl T. Boone
The Aerospace Corporation, El Segundo, CA

We report the performance of an all-fiber-connected telecom wavelength entangled photon source with both high-rate pulsed and continuous wave seed lasers in terms of coincidence count rate and Hong-Ou-Mandel visibility and test optimization schemes based on low-frequency noise reduction. Using a noise eater after the seed laser, the coincidence count rates for a 200ps coincidence window are measured to be 1335 (CW) / 1226 (pulsed) count/second/mW and visibilities are 80.6% (CW) / 87.4% (pulsed).

27.2: Rydberg Atomic Electric Field Sensor and Receiver (1:55)

He Wang, David Rosser, Carl T. Boone
The Aerospace Corporation, El Segundo, CA

We report a cesium (Cs) atomic microwave sensor and receiver and its applications for electric field (E-field) sensing and data transmission. The sensor system is associated with Cs Rydberg transitions at various frequencies, which is generated with double-resonance laser excitations. In this work, we used the Electromagnetically Induced Transparency (EIT) and Autler-Townes (AT) effects to measure radio frequency (RF) E-field strengths in both strong field and weak field regime and experimentally studied the system's temporal responses as a receiver to amplitude, frequency, and phase shift keying modulations for data transmission. Modeling shows that Cs atoms have accessible Rydberg transitions at frequencies ranging from MHz to THz for sensing and communication applications.

27.3: A Quantum Magnetic Microscope for Electronics Diagnostics (2:20)

Jennifer M. Schloss, Pauli Kehayias, Rohan Kapur, Danielle A. Braje
MIT Lincoln Laboratory, Lexington, MA

Effective technologies to ensure microelectronics fabrication process robustness and safeguard resultant systems are critical to keep pace with increasingly complex US needs. Existing diagnostic tools can be slow, invasive, delicate, or unable to pinpoint anomaly locations. Widefield magnetic microscopy using quantum nitrogen-vacancy (NV) centers in diamond allows for noninvasive spatial localization of electrical currents. Magnetic imaging circumvents limitations of other techniques, especially in visualizing anomalies in opaque, interconnected integrated circuits. Moreover, the NV microscope's optical readout illuminates spatiotemporal dynamics inaccessible to scanning microscopy techniques. This technique has already shown success identifying faults, hardware trojans, and other circuit anomalies. Still, previous works have focused on imaging static signals. Using a quantum frequency mixing technique, we image currents at frequencies up to 70 MHz across a >1 mm^2 field of view. This added versatility further positions NV magnetic microscopy an effective tool for microelectronics failure analysis, supply chain security, and fabrication process characterization.

27.4: Scheduling Satellites Using Quantum Computers (2:45)

John P. T. Stenger, C. Stephen Hellberg, Daniel Gunlycke, Kelly Harnish
U.S. Naval Research Laboratory, Washington, DC

There is an ever increasing number of satellites in orbit and there are often large arrays of targets that need to be imaged. We aim to find an optimized schedule that determines which satellites should image which targets. Quantum computers may have an advantage over classical computers for optimizing satellite schedules. In order to achieve this advantage, we must (1) derive an encoding that maps the satellite schedules to the state space of the quantum computer and (2) create a quantum algorithm that finds the optimal schedule. We present several encodings to map the satellite schedules to the state of the quantum computer. We also present a variational algorithm for optimizing the schedules using a quantum computer. We demonstrate the algorithm on an IBM quantum computer.

BREAK (3:10–3:30)

SHIP-STEAMpipe

Wednesday, March 19 / 1:30–3:10 pm / Ballroom B

Chair: **Brian Olson**
Department of the Navy Crane, Crane, IN

Co-Chair: **Christopher Riso**
Booz Allen Hamilton, McLean, VA

28.1: Thermal Test Vehicles for Characterization of Next Generation Heterogenous Packaging Utilizing Glass Core Substrates **(1:30)**

Matthew Irvine, Andrew Ketterson, Anthony Chiu, Kirk Ashby, Corey Slattum
Qorvo, Richardson, TX

Joe Proulx
Siemens, Marlborough, MA

28.2: Glass Substrate-Based 3D RF System-in-Package: SHIP RF Advanced Technology Use Case **(1:50)**

Sarah Woodworth, David Shahin, Matthew Doerflein, Aaron Wescott, Waseem Ahmed, Michael Langlois, Maxim Serebreni, Adam Rusenko, Sara Taylor
Northrop Grumman Mission Systems, Baltimore, MD

28.3: UCIe Enabled MCP for Next Generation Arrays **(2:10)**

Ted Hoffmann, Jason Kehl
Raytheon, Hanover, MD and El Segundo, CA

Dagan White, Scott Norrholm
AMD, San Jose, CA

Robert Keller, Collin Wells, Tommy Neu
TI, Dallas, TX

28.4: Next Generation Bits-to-RF Design for State-of-the-Art Heterogeneous Integrated Packaging (SHIP) **(2:30)**

Spencer Pace, Rajanish Pandey, Indy Chatterji
Qorvo, Richardson, TX

Paul Mosinskis
Cadence Design Systems, San Jose, CA

This paper will present the comprehensive design methodology of the next generation of co-simulation design flow being developed under the SHIP RF program. It will cover the existing state of the design flow and the addition of true mixed signal, digital/RF co-simulation capabilities. A X-band front end module (FEM) is used to depict the enablement of tools and communication protocol to outline the design steps. Electrical, mechanical and thermal aspects will be demonstrated. Then an integrated mixed signal exemplar of a digitally controlled phased array will be presented in detail to showcase the simulated electrical, electromagnetic, and radiated results. After presenting the full path for design capture, analysis, and verification, an assembly overview for the phased array design will be presented.

28.5: Workforce Development Needs in Heterogeneous Integration and Advanced Packaging: DoD SCALE Program **(2:50)**

Jakob Isaiah Ramos, Steve Shade, Gabriella Torres, Amy Marconnet, Kerrie Douglas, Peter Bermel, Ganesh Subbarayan, Shubhra Bansal
Purdue University, West Lafayette, IN

Matthew Krinick, Roa Fernando
Booz Allen Hamilton, McLean, VA

Muhannad Bakir
Georgia Institute of Technology, Atlanta, GA

Scott Schiffres
Binghamton University State University of New York, Binghamton, NY

Dhruv Bhate
Arizona State University, Mesa, AZ

BREAK **(3:10–3:30)**

FILTER TECHNOLOGY

Wednesday, March 19 / 1:30–3:10 pm / Ballroom C

Chair: Timothy Hancock
Raytheon Technologies, Tewksbury, MA

Co-Chair: Adilson Cardoso
Raytheon, Atlanta, GA

29.1: UHF/VHF Band Auto-tune Filter Development (1:30)

William Wilber, Scott Gillette
Metamagnetics, Inc., Marlborough, MA

29.2: Design and Power Handling of X- and Ku-Band AlScN Resonator-Based Filters (1:50)

Sean Yen, Christopher D. Nordquist, Zachery M. Woods, Tyler A. Liebsch, David Krawczyk, Giovanni Esteves
Sandia National Laboratories, Albuquerque, NM

Pinal Patel, Craig Moe, Mojtaba Hodjat-Shamami, Daeho Kim, Ramakrishna Vetury
Akoustis Technologies, Inc., Huntersville, NC

We show the design and power handling of X- and Ku-band bandpass filters fabricated in aluminum scandium nitride bulk acoustic wave technology. Power handling test results show permanent failure at 28.4 dBm of input power, with the outermost resonators failing at the band edge frequencies. Any notable results from a power mitigation technique being tested will be shared in the full paper.

29.3: Enabling Fast Steering of Arbitrary Spatial Filters with Phased Arrays (2:10)

Arun Paidimarri, Bodhisatwa Sadhu, Alberto Valdes-Garcia
IBM T.J. Watson Research Center, Yorktown Heights, NY

Phased array-based systems must support the formation of spatial filters with precise lobes and nulls in specific locations to operate effectively in complex environments with multiple users, objects, and interferers. Additionally, the ability to switch between different spatial filter configurations rapidly is highly desirable. Current methods for fast beam steering are either constrained by the limited memory capacity of RF front-ends or are restricted to fast steering of beams with sinc-shaped patterns. In this work, we present a novel approach for enabling the rapid steering of arbitrary spatial filters. Our method involves defining a spatial filter in the broadside direction and steering it through a transformation process. Simulation results validate the effectiveness of this technique, showcasing steering of beams with spatial notches, wide-lobed beams, and multi-pronged beams. An experimental demonstration is currently underway, and measurement results will be included in the final version of this paper.

29.4: An Autonomous Near Real Time Spin Wave-Based Analog Frequency Selective Canceller (2:30)

Randy Camasso, Reena Dahle, Scott Gillette
Metamagnetics, Marlborough, MA

29.5: Total Spectrum Filtering: A First Look at Multi-Octave Frequency Reconfigurability **(2:50)**

Matthew Torpey, Andrew Bothelho, Taylor Brown, Andras Resch, Jonathan Egan, Sean McLoughlin
Northrop Grumman Mission Systems, Linthicum, MD

BREAK **(3:10–3:30)**

Session 30 (TA10 – Trusted, Assured and Cyber-secure Microelectronics)

SIDE CHANNELS AND SIGNAL ANALYSIS

Wednesday, March 19 / 1:30–3:10 pm / Ballroom D&E

Chair: Christian Eakins
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: Jamin McCue
Air Force Research Laboratory, Wright-Patterson AFB, OH

30.1: TPUXtract: A Comprehensive Hyperparameter Stealing Framework on Edge TPUs (1:30)

Ashley Kurian, Anuj Dubey, Aydin Aysu
North Carolina State University, Raleigh, NC

Model stealing attacks on AI/ML devices undermine intellectual property rights, compromise the competitive advantage of the original model developers, and potentially expose sensitive data embedded in the model's behavior to unauthorized parties. While previous works have demonstrated side-channel-based model recovery in embedded microcontrollers and FPGAs, the exploration of attacks on commercial ML accelerators remains largely unexplored. This paper demonstrates the first successful model extraction attack on the Google Edge Tensor Processing Unit, an off-the-shelf ML accelerator. Specifically, we show a hyperparameter stealing attack that can extract all layer configurations. Most notably, our attack is the first comprehensive attack that can extract previously unseen models. This is achieved through an online template-building approach instead of a pre-trained ML-based approach used in prior works. Our results show that, through obtained electromagnetic traces, our proposed framework can achieve 99.91% accuracy, making it the most accurate one to date. Our findings call for countermeasures.

30.2: Side-Channel-Attack-Resilient Asynchronous Polymorphic Cryptographic Circuit in 12 nm FinFET (1:50)

Richard Becker, Zhihan Weng, Kelby Haulmark, Nicholas Brown, Kyle Orman, Jia Di
University of Arkansas, Fayetteville, AR

Cryptographic hardware plays a pivotal role in establishing roots of trust to uphold security requirements in modern computing environments. However, many implementations of cryptographic algorithms are susceptible to side-channel attacks (SCA), as well as a host of other threat vectors, which can expose sensitive information. This paper details the physical implementation and testing of an asynchronous polymorphic circuit (APC) whereby the supply voltage provided to the chip dictates one of its two functionalities. At the high supply voltage, the APC functions as a SHA3-512 core; at the low supply voltage, the chip instead functions as an AES-256 core. This polymorphism is implemented with a secure asynchronous logic paradigm to enhance resilience against side-channel attacks by perfectly balancing the switching activities across different data patterns. The design was fabricated using the GlobalFoundries 12 nm FinFET process, and the dies were packaged and tested to verify the polymorphic behavior on silicon. A –0.4355 score of Welch's t-test demonstrates the APC's resilience to SCAs.

30.3: Hardware Moving Target Defenses against Post-Silicon Side-Channel Leakages (2:10)

Saleh Khalaj Monfared, Kyle Mitard, Shahin Tajik
Worcester Polytechnic Institute, Worcester, MA

Domenic Forte
University of Florida, Gainesville, FL

Side-channel vulnerabilities pose significant risks to the security of cryptographic implementations on integrated circuits. These vulnerabilities stem from the natural effects of computation and data storage, which impact factors such as power consumption and supply voltage fluctuations within the IC. These leakage characteristics have been exploited in various side-channel analysis attacks, enabling breaches in the security of cryptographic systems. Despite the some mitigation efforts, cryptographic chips remain vulnerable to new sophisticated class of physical attacks such as impedance analysis, optical probing, or even electron beams. These analysis allow the attackers to extract sensitive information from the chip. This article propose a systematic defense against advanced physical attacks. We describe a Moving Target Defense (MTD) approach on the hardware, as a real-time and adaptive response to SCAs targeting the chips. We implement a MTD prototype on a FPGA via partial reconfiguration and evaluate it against multiple advanced physical attacks.

30.4: Securing Cryptographic Hardware: Detecting and Mitigating Power Side-Channel Attacks (2:30)

Amisha Srivastava, Kanad Basu
University of Texas at Dallas, Richardson, TX

Power side-channel (PSC) attacks, which exploit dynamic power consumption in cryptographic hardware, pose significant security risks by enabling the extraction of sensitive information. Traditional countermeasures, such as masking schemes, often encounter challenges, including complex integration and the risk of compromised security features during synthesis. We propose a novel approach that combines pre-silicon PSC analysis with side-channel-aware logic synthesis to address these limitations. Our method uses a graph neural network to convert RTL designs into control-data flow graphs, identifying and mapping vulnerable modules to standard cells with minimal PSC leakage. When evaluated using cryptographic benchmarks like AES, RSA, and post-quantum cryptography algorithms, our approach achieves up to 94.49% localization accuracy, reduces attack success rates to as low as 9%, and improves area efficiency by up to 3.79X compared to traditional methods. This integrated solution enhances cryptographic hardware security, leading to faster design closure and reduced costs.

30.5: Effects of Injected Signal Properties on Power Spectrum Analysis for Recycled FPGA Detection (2:50)

Frank T. Werner, Christopher R. Clark
Georgia Tech Research Institute, Georgia Institute of Technology, Atlanta

The detection of recycled FPGAs is a serious concern for the microelectronics industry. They have a shortened lifespan and can cause the systems that rely on them to fail prematurely. Given its simplicity, power spectrum analysis (PSA) is an attractive option for recycled FPGA detection. However, the PSA measurements need to be carefully designed to be able to detect the small differences between new and recycled FPGAs. Currently little research has been published on how the properties of the injected signal used for PSA impact the accuracy. For simple devices, the properties are not as strict since the response is easy to model. On the other hand, as this work demonstrates, for more sophisticated ICs, such as FPGAs, the duty cycle, frequency, and amplitude of the injected signal have a significant impact on PSA's accuracy.

BREAK (3:10–3:30)

OPTIMA

Wednesday, March 19 / 1:30–3:10 pm / Ballroom H

Chair: **Todd Bauer**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Jonathan Hoffman**
Army Research Lab, Adelphia, MD

31.1: CIMPool: Scalable Neural Network Acceleration for Compute-In-Memory Using Weight Pools **(1:30)**

Shurui Li, Ravit Sharma, Puneet Gupta
University of California, Los Angeles, Los Angeles, CA

31.2: Back-Gate Mediated V_{TH} Mismatch Reduction to Enable 6-bit Precision in FD-SOI Charge-Trap Transistors **(1:55)**

Siyun Qiao, Samuel Wang, Ziyi Guo, Mohammadreza Zeinali, Vinod Kurian Jacob, Samyak Chakrabarty, Subramanian S. Iyer, Sudhakar Pamarti
University of California, Los Angeles, Los Angeles, CA

Jacklyn Zhu
Columbia University, New York, NY

Boris Vaisband
University of California, Irvine, Irvine, CA

31.3: Switched Capacitor In-Memory Computing (IMC) for Scalable AI Systems **(2:20)**

Naveen Verma
Princeton University, EnCharge AI, Princeton, NJ

Kailash Gopalakrishnan, Echere Iroaga
EnCharge AI, Santa Clara, CA

In-memory computing (IMC) is a critical technology for addressing energy and performance limitations of running state-of-the-art AI workloads in today's computing systems. This paper focuses on switched-capacitor (SC) IMC, which has demonstrated the highest efficiency and accuracy to date, describing the fundamental technology and its integration into full computing systems, under the DARPA OPTIMA program. The team consists of researchers from Princeton University, who first introduced SC IMC technology, and the startup EnCharge AI, which is developing advanced AI computing products for the commercial and defense ecosystems. This project draws from previous works to explore the limits of SC IMC and push its implementations towards those limits at the technology/circuit level (through scaling to advanced CMOS nodes as well as by developing optimized ADC and power-delivery architectures), and at the architectural level (through supports and codified application-mapping policies for flexible parallelism, as well as quantization tools for maximizing accuracy).

31.4: Robust Energy-Efficient Sensor Platform using Analog Feature Extraction and Local Restoration **(2:45)**

Isha Chakraborty, Jongseok Woo, Minah Lee, Wei-Chun Wang, Narasimha Vasishta Kidambi, Sharadindu G. Kirtania, Eknath Sarkar, Khandker A. Aabrar, Dyutimoy Chakraborty, Suman Datta, Saibal Mukhopadhyay
Georgia Institute of Technology, Atlanta, GA

Analog Feature Extraction (AFE) and Local Feature Restoration (LFR) enable a robust energy-efficient sensor platform. AFE preprocesses and reduces dataset to minimize communication overhead, while LFR restores noisy features from analog compute noise. Compared to baseline, the platform provides 50.4–70.8% energy savings with 10.5% (0.3%) accuracy degradation for ImageNet200 (CIFAR10) and less than 2% LFR area/energy overhead.

BREAK **(3:10–3:30)**

ADVANCED POWER ELECTRONICS

Wednesday, March 19 / 1:30–3:10 pm / Ballroom G

Chair: **Michael Mastro**
U.S. Naval Research Laboratory, Washington, DC

Co-Chair: **Travis Anderson**
University of Florida, Gainesville, FL

32.1: Enabling Future Ultra-Wide Bandgap (UWBG) and Extreme WBG (EWBG) Power Electronic Building Blocks (PEBB) **(1:30)**

Lynn Petersen
Office of Naval Research, Arlington, VA

32.2: High Density Power Electronics in Aerospace and Defense Applications **(1:50)**

Parag Kshirsagar, Jeffrey Ewanchuk
RTX Technology Research Center (RTRC), East Hartford, CT

Erin Nolan
Raytheon, Marlborough, MA

This paper highlights the high-power density and efficient electrification components in commercial aviation comprising of power generation, distribution, propulsion, and storage system and attempts to map those metrics with emerging defense applications for space, aerospace, terrestrial, and naval power systems.

32.3: 100 mm Bulk AlN Substrates for Next Generation UWBG Electronics **(2:10)**

Kasey Hogan, Robert T. Bondokov, James Grandusky, Shogen Matsumoto, Griffin Q. Norbury
Crystal IS, Inc., Green Island, NY

There is an ever-increasing need for robust devices in defense and commercial applications with high power density, high voltage capability, and high frequency capability, which can withstand high junction temperatures (>200 C). Bulk AlN substrates look to enable such electronic devices due to the high thermal conductivity, ultrawide bandgap, close lattice matching with other III-N ($Al_xGa_{1-x}N$), and low dislocation density. AlN boules are grown using Physical Vapor Transport (PVT) technique, with a diameter sufficient for the fabrication of 100 mm AlN substrates. Double-axis X-ray diffractometry (XRD) rocking curves shows full width at half maximum (FWHM) values of <50 arcsec, while etch pit density (EPD) indicates defect density ~10^4 cm^{-2}. The single-crystal area measured by high-resolution cross-polar imaging (HRCPI) exceeds 99%. These results along with its high thermal conductivity make the 100 mm AlN material a great candidate for use as a substrate for next generation photonic and electronic devices.

32.4: High Operating Temperature AlGaN-Channel HEMTs Enabled by Regrown Reverse-Graded Ohmic Contacts **(2:30)**

Brianna Klein, Andrew Allerman, Andrew Armstrong, Troy Tharpe, GlenAsia Gonzalez, Eric Cruz, Giovanni Esteves
Sandia National Laboratories, Albuquerque, NM

James Spencer Lundh, Marko Tadjer
U.S. Naval Research Laboratory, Washington, DC

Roy Olsson
University of Pennsylvania, Philadelphia, PA

Semiconductor switches capable of operating in temperatures beyond the reach of conventional semiconductors, such as silicon, are needed for applications including geothermal wells, automotive, and hypersonic systems. Al-rich AlGaN transistors are excellent candidates for extreme temperature operation due to their ultra-wide bandgaps, which simultaneously promote large Schottky barrier heights that minimize gate leakage and discourage deleterious intrinsic carrier effects. However, a major challenge facing AlGaN transistors is the fabrication of low resistance Ohmic contacts. Recently, regrown compositionally reverse-graded contacts to $Al_{0.85}Ga_{0.15}N$-barrier/$Al_{0.68}Ga_{0.32}N$-channel transistors with average specific contact resistances of 1.8×10^{-4} $\Omega \cdot cm^2$ have been developed. We have subjected such transistors to in-situ DC testing up to 650 °C (in vacuum) and measured a 35% decrease in saturation drain current compared to room temperature data. We have observed a full recovery of drain current upon return to room temperature. These results show a promising approach to fabricating AlGaN transistors for extreme temperature applications.

32.5: Engineered Layers and Substrates for High Power Electronics **(2:50)**

Mark S. Goorsky, Brandon Carson, Kaicheng Pan
UCLA Materials Science and Engineering, Los Angeles, CA

Michael E. Liao
APEX Microdevices, West Chester, OH
and
UCLA Materials Science and Engineering, Los Angeles, CA

Kenny Huynh
Information Sciences Institute, University of Southern California, Marina Del Rey, CA

Piyush Shah
APEX Microdevices, West Chester, OH

The heterointegration of wide and ultra-wide bandgap materials for high power electronics, including thermal management, band structure optimization, and other aspects can be achieved using techniques that include but also go beyond epitaxial deposition. Here, we describe some important wide bandgap combinations achieved through wafer bonding / fusion / layer transfer / as well as deposition to demonstrate how control of interfaces can lead to better multi-layer performance and also how thermal transport models can be applied to these novel systems to lead to improvements in combined electronic and thermal management performance. The development and design of engineered substrates provides another means to enhance performance for power electronics. Examples include bonding using diamond, GaN-AlN bonding across N-face and metal face interfaces, and β-Ga_2O_3. The importance of understanding interface preparation for both bonding and deposition applications, exfoliation techniques, as well as judicious introduction of thin interfacial layers will be described.

BREAK **(3:10–3:30)**

PIC-BASED PROCESSING AND COMPUTING

Wednesday, March 19 / 1:30–3:10 pm / Ballroom F

Chair: **Jim Adleman**
SPAWAR, San Diego, CA

Co-Chair: **Steven Palmer**
NIST, Gaithersburg, MD

33.1: Design of Energy-Efficient Photonic SRAM for High-Speed On-Chip Photonic Memory Systems (1:30)

Md Abdullah-Al Kaiser, Akhilesh R. Jaiswal
University of Wisconsin-Madison, Madison, WI

Sugeet Sunder, Ajey P. Jacob
University of Southern California, Information Sciences Institute, Marina del Rey, CA

Michal Rakowski
GlobalFoundries, Malta, NY

In this work, we propose a novel photonic static random access memory (pSRAM) design using fabrication-friendly photonic components. The proposed pSRAM overcomes the key limitations of traditional electrical SRAMs, which struggle with speed and power efficiency due to increasing bitline/wordline capacitance and interconnect resistance associated with long electrical wires as technology scales. By utilizing cross-coupled micro-ring resonators and differential photodiode structures, along with optical waveguides instead of traditional wordlines and bitlines, our pSRAM exhibits high-speed, and energy-efficient performance. The pSRAM bitcell achieves a read/write speed of 20 Gbps with energy consumption of around 1.0 pJ/bit and a 0.1 mm^2 footprint in the GF45CLO PDK. These bitcells can be arranged into a 2D memory array, enabling large-scale, on-chip photonic memory subsystems ideal for high-speed memory and computing applications.

33.2: Leveraging Photonic Interconnects for Scalable and Efficient Fully Homomorphic Encryption (1:50)

Dewan Saiham, Di Wu, Sazadur Rahman
University of Central Florida, Orlando, FL

Fully Homomorphic Encryption (FHE) is a key technology enabling privacy-preserving computing on encrypted data. However, the practical usage of FHE is critically limited due to its high computation complexity, extremely intensive memory access, and limited generality. Existing hardware accelerators designed for FHE mostly focus on compute acceleration alone and encounter performance bottlenecks due to high memory access and complex dataflow challenges. This paper introduces a scalable photonic interconnect network to enhance the efficiency of FHE accelerators by addressing the issues related to intricate memory access patterns in Number Theoretic Transform (NTT) computations. The proposed solution leverages the advantages of photonic communication to optimize data transfer and processing, thereby offering a more scalable and effective approach to handling the computational demands of FHE.

33.3: Novel Optical In-memory Compute Engine (2:10)

Sugeet Sunder, Clynn J. Mathew, Ajey P. Jacob
University of Southern California, Information Sciences Institute, Marina del Rey, CA

Md Abdullah-Al Kaiser, Akhilesh R. Jaiswal
University of Wisconsin Madison, Madison, WI

Sasindu Wijeratne, Viktor Prasanna
University of Southern California, Los Angeles, CA

Michal Rakowski
GlobalFoundries, Malta, NY

Breaking the von Neumann bottleneck, we present a revolutionary in-memory optical compute processor chip that integrates high-speed photonic SRAM (>20 GHz) with optical analog computing. This groundbreaking design eliminates separate processing and memory units, dramatically reducing latency and energy consumption. Our chip combines 16-level, 4-bit input optical analog computing with 4-bit digital memory control, achieving high-fidelity 8-bit output. Scalable through dense wavelength division multiplexing, it enables massive parallelism via hyperspectral encoding. This fusion of optical and digital technologies paves the way for ultra-efficient, high-performance computing in artificial intelligence and scientific applications. We're also developing a hardware-algorithm co-design architecture optimized for the Matricized Tensor Times Khatri-Rao Product (MTTKRP), a critical kernel in tensor decomposition. Join us as we illuminate the future of computing, where light becomes the medium for unprecedented computational power and efficiency.

33.4: Dynamic Optical Switching Using Phase-Change Materials in Double Micro-Ring Resonators for Neuromorphic Computing (2:30)

Sarah S. Sharif, Yaser Mike Banad
School of Electrical and Computer Engineering, University of Oklahoma, Norman, OK

This paper presents a novel design for a double micro-ring resonator utilizing $Ge_2Sb_2Te_5$ (GST) phase-change materials for applications in optical neural networks. By leveraging the unique properties of GST, the proposed resonator demonstrates temperature-dependent nonlinear activation functions, enabling precise control of light transmission for high-performance switching. The device's design incorporates two coupling regions and a rectangular waveguide, and the resonator's transmission characteristics are thoroughly analyzed using Finite Difference Time Domain (FDTD) simulations. Key performance metrics such as Full Width at Half Maximum (FWHM), Quality Factor (Q-factor), and Free Spectral Range (FSR) are investigated, demonstrating the device's tunability through GST angular orientation and temperature modulation. The study highlights the potential of this design for optical neuromorphic systems by enabling dynamic transmission control, making it a promising candidate for optical switching and filtering applications within the telecommunication wavelength range.

33.5: Boosting Near-Sensor Visual Processing with Silicon-Photonics-Enabled Edge Intelligence (2:50)

Mehrdad Morsali, Deniz Najafi, Shaahin Angizi
New Jersey Institute of Technology, Newark, NJ

Mahdi Nikdast
Colorado State University, Fort Collins, CO

Enhancing image sensors for real-time classification and deep neural network (DNN) acceleration can significantly advance various application domains (autonomous systems, surveillance and security, drones, augmented reality (AR), etc.). This abstract paper summarizes our recent work on employing silicon photonic neural networks on image sensors, to achieve high energy efficiency and computational performance for near-sensor visual processing. By developing an efficient photonic hardware-software co-design and cross-layer co-optimization approach, we demonstrated the first optical near-sensor processing systems, called OISA and Lightator, achieving an average reduction in power consumption by a factor of approximately 24× and 73× compared with existing photonic accelerators and GPU baselines.

BREAK (3:10–3:30)

IN MEMORY/SENSOR COMPUTATION

Wednesday, March 19 / 3:30–4:50 pm / Ballroom A

Chair: **Ezra Hall**
GlobalFoundries, Essex Junction, VT

Co-Chair: **Shawn Fetterolf**
Intel, Santa Clara, CA

34.1: High-Density FeFET-Based CAM Cell Design (3:30)

Rouwaida Kanj
Synopsys, Inc., Austin, TX

Omar Bekdache
University of Illinois Urbana-Champaign, Urbana, IL

Hadi Noureddine
Technical University of Munich, Munich, Germany

Mohammed Fouda
Rain Neuromorphics, San Francisco, CA

Ahmed Eltawil
KAUST, Thuwal, Saudi Arabia

Due to their inherent parallel search capability, content addressable memories (CAM) lend themselves as an ef-fective solution for numerous applications such as net-work-routing and neuromorphic associative memory. In this paper, we present multi-level FeFET CAM design solutions with enhanced storage capabilities. We first explore 2T complementary FeFET CAM design and evaluate its performance compared to its n-type counterparts for multi-bit cell storage. With process variations limiting the number of reliable FeFET program-able states, we explore exploiting multi-level FeFETs using more transistors per cell and develop a multi-dimensional encoding scheme for enhanced cell storage. This work paves the way for denser storage and higher energy efficiency systems.

34.2: Enabling Future Flight Systems with Analog In-Memory Processing (3:50)

Sapan Agarwal, David Richardson, Ben Feinberg, Denis Ridzal, Aurya Javeed, Drew P. Kouri, David R. Hughart, Nad Gilbert, T. Patrick Xiao, Christopher Bennett
Sandia National Laboratories, Albuquerque, NM

Matthew J. Marinella
Arizona State University, Phoenix, AZ

34.3: Analog Computing Using SONOS Charge Trap Memory for Low-Power Space-Borne Artificial Intelligence **(4:10)**

T. Patrick Xiao, Christopher H. Bennett, William Wahby, Park Hays, David R. Hughart, Sapan Agarwal
Sandia National Laboratories, Albuquerque, NM

Vineet Agrawal
Infineon Technologies, San Jose, CA

Matthew J. Marinella
Arizona State University, Tempe, AZ

Real-time intelligent processing of data streams from large, high-speed focal plane arrays requires hardware that can deliver high-performance, low-power processing on a satellite. We present an analog in-memory computing prototype based on 40 nm SONOS charge-trap memory that can accurately and efficiently process artificial intelligence (AI) workloads for space remote sensing, and characterize its sensitivity to space radiation.

34.4: FPCA: Field-Programmable Pixel Convolutional Array for Extreme-Edge Intelligence **(4:30)**

Zihan Yin, Md Abdullah-Al Kaiser, Akhilesh Jaiswal
University of Wisconsin-Madison, Madison, WI

Advancements in neural network applications require hardware that accelerates computation and adapts to dynamic processing needs. While processing-in-pixel offers a solution to extreme-edge bottlenecks, existing designs lack reconfigurability and scalability due to their static nature and inefficient area usage. We introduce a novel architecture that enhances processing-in-pixel capabilities for convolutional neural networks. By integrating non-volatile memory with a new pixel circuit design, we enable dynamic reconfiguration of synaptic weights, kernel size, channel size, and stride size, providing exceptional flexibility. Using a separate die for the pixel circuit and synaptic weight storage significantly reduces the area per pixel, boosting the density and scalability of the pixel array. This work addresses current limitations and opens new avenues for efficient, flexible, and scalable neural network hardware, paving the way for advanced AI applications.

EVENING SOCIAL (OFFSITE) **(6:00–10:00)**
(Buses begin leaving at 5:00 pm)

SHIP – MULTI-CHIP PACKAGING

Wednesday, March 19 / 3:30–4:50 pm / Ballroom B

Chair: **Brian Olson**
Department of the Navy Crane, Crane, IN

Co-Chair: **Saverio Fazzari**
Booz Allen Hamilton, Washington DC

35.1: Project Day Watch: Environmental Test Plan for SHIP's MCP-1 Prototypes **(3:30)**

Ruth Hidalgo-Hernandez, Aaron Clough-Paez, Laura Jean Weidman, Jason O'Brien, Allison Hill
Department of Defense, Fort Meade, MD

35.2: Advanced Packaging and Test Technical Execution Area Technology Transition Best Practices **(3:50)**

Brian D. Olson
Naval Surface Warfare Center, Crane Division, Crane, IN

35.3: Flight Test Results for SHIP Wideband Integrated Flight Test (SWIFT) **(4:10)**

Jon Wagner, David Pawlowicz, Ed Terry, Jason Bensaull
Lockheed Martin, Owego, NY

35.4: OUSD SHIP MCP Program Evolution **(4:30)**

Carmine Pagano
Altera Corporation, Parsippany, NJ

Ben Esposito
Altera Corporation, Raleigh, NC

John Sotir
Altera Corporation, Kennebunkport, ME

EVENING SOCIAL (OFFSITE) **(6:00–10:00)**
(Buses begin leaving at 5:00 pm)

WARP

Wednesday, March 19 / 3:30–5:10 pm / Ballroom C

Chair: **Todd Bauer**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Steven Gross**
DARPA MTO SETA, Arlington, VA

36.1: Tunable GaN / Bulk Acoustic Wave Bandpass Filters **(3:30)**

Matthew Morton, Charles Wang, William Sear, Jason Adams, Adam Peczalski, Matt Rebholz, Diana Fayngersh Lee, Wayne Hobby
Raytheon Technologies, Andover, MA

Damla Dimlioglu, Thomas Tapen, Alyosha Molnar, Alyssa Apsel
Cornell University, Ithaca, NY

36.2: Tunable Notch Filters Based on GaN Gyrators **(3:50)**

Matthew Morton, Charles Wang, William Sear, Jason Adams, Adam Peczalski, Matt Rebholz, Diana Fayngersh Lee, Wayne Hobby
Raytheon Technologies, Andover, MA

Armagan Dascurcu, Nishant Patil, Nusrat Jahan, Harish Krishnaswamy
Columbia University, New York, NY

36.3: Zero Static Power, High-Q Magnetostatic Wave Filters with Enhanced Frequency Tuning Range **(4:10)**

Xingyu Du, Yixiao Ding, Shun Yao, Zhehao Yu, Alexander J. Geers, Firooz Aflatouni, Mark Allen, Roy H. Olsson III
University of Pennsylvania, Philadelphia, PA

Recently magnetostatic wave bandpass and bandstop filters that are frequency tunable from 3.3–11.1 GHz using a miniature, zero static power, magnetic bias circuit have been reported. This paper describes updates to the technology that extends the frequency tuning range from 2–17 GHz while reducing the overall filter size to 1.2 cc. The frequency tuning range of 8.5:1 greatly exceeds that achieved using tuning approaches based on RF MEMS or varactors, while the power consumption and volume are orders of magnitude lower than commercial tunable magnetostatic wave filters based on yttrium iron garnet (YIG) spheres.

36.4: Self Interference Cancellation using a Photonic-Acoustic Network on Commercial SOI SiPh Process **(4:30)**

Mertcan Erdil, Izhar FNU, Yang Deng, Ella Klein, Roy H. Olsson III, Firooz Aflatouni
University of Pennsylvania, Philadelphia, PA

We report progress on development of an integrated photonic-acoustic system to perform self-interference cancellation in wideband RF transceivers. Preliminary measurement results are reported.

36.5: Compact Magnetostatic-wave Resonators at W-band **(4:50)**

David Connelly
Metamagnetics, Inc., Marlborough, MA

EVENING SOCIAL (OFFSITE) **(6:00–10:00)**
(Buses begin leaving at 5:00 pm)

Session 37 **(TA10 – Trusted, Assured and Cyber-secure Microelectronics)**

PRIVACY ENHANCING TECHNOLOGIES (PET)

Wednesday, March 19 / 3:30–4:50 pm / Ballroom D&E

Chair: **Bryan Jacobs**
DARPA MTO, Arlington, VA

Co-Chair: **Johnny Marsh**
DARPA MTO SETA, Arlington, VA

37.1: Combating Hardware Trojans in Secure Designs (3:30)

Adam Sherer, Asha Rai, Daniel Murray
Cadence Design Systems, Burlington, MA

Matthew D. Sale
Air Force Research Laboratory, WPAFB, OH

Austin Vorst, Mark Labbato
Booz Allen Hamilton, Beavercreek, OH

Hardware Trojans and other exploitable weakness can affect the confidentiality, integrity, and availability of a system. The ability to make data-driven readiness decisions with respect to increasingly complex defense systems requires abstraction and continuous traceability throughout the development cycle. Metric Driven Verification (MDV) strengthens defense systems by implementing an executable verification plan with measurable goals and providing traceability from metrics to requirements. Integrating this plan into the regression management tool allows for a structured assessment of the progress. Regression management tools that combine coverage from multiple engines, such as simulation and formal analysis allow for a more efficient design assurance effort. This systematic approach allows for continuous tracking of progress, and creation of standardized reports. This paper demonstrates a Rapid Adoption Kit (RAK) that serves as a cookbook for guiding the efforts of performers to speed design verification development and closure.

37.2: Accelerating FHE to Enable Privacy-Preserving Deep Learning (3:50)

Ahmad Al Badawi, Yuriy Polyakov, Ronen Cohen, Carlo Pascoe, Sarabjeet Singh, David Bruce Cousins, Kurt Rohloff
Duality Technologies, Hoboken, NJ

Matthew French, Benedict Reynwar, Troy Hicks, Kellie Canida, Clynn Mathew, Ajey Jacob, Kenneth M. Zick
USC, Information Sciences Institute, Arlington, VA

Akshath Mahajan, Mukund Ramakrishnan, Rugved Mhatre, Austin Ebel, Brandon Reagen
New York University, New York, NY

37.3: BASALISC: Programmable Hardware Accelerator for CKKS, BGV, and BFV Fully Homomorphic Encryption **(4:10)**

David W. Archer, James LaMar, Iavor Diatchki
Galois, Inc., Portland, OR

Georgios Dimou, Tynan McAuley
Niobium Microsystems, Dayton, OH

Robin Geelen, Michiel Van Beirendonck, Hilder V. L. Pereira, Ingrid Verbauwhede, Frederik Vercauteren
KU Leuven, Leuven, Belgium

37.4: Fully Homomorphic Encryption with Safe Disclosures **(4:30)**

Todd Austin
University of Michigan, Ann Arbor, MI

Alex Kisil
Agita Labs, Inc, Ann Arbor, MI

Brandon Reagen
New York University, New York, NY

Fully Homomorphic Encryption (FHE) offers a powerful tool for ensuring privacy by allowing computations on encrypted data without requiring decryption. This form of computation protects the data throughout its lifecycle, even during processing. However, while FHE can solve many privacy concerns, it remains impractical in adversarial sharing environments where distrustful parties need to compute on shared data. This work addresses adversarial sharing challenges by introducing a hardware-enforced solution that extends FHE computation to ensure secure and verifiable computations between distrustful parties. It combines FHE with dataflow hashing and proxy re-encryption within a secure hardware enclave, ensuring that computations on encrypted data are tamper-proof and that only authorized results can be disclosed. This solution enables secure applications such as credit risk assessment and regulatory monitoring, ensuring that both parties can trust the computations and their results, even in adversarial settings.

EVENING SOCIAL (OFFSITE) **(6:00–10:00)**
(Buses begin leaving at 5:00 pm)

RADIATION HARDENED BY DESIGN (RHBD)

Wednesday, March 19 / 3:30–4:50 pm / Ballroom H

Chair: Lloyd Massengill
Reliable MicroSystems, Franklin, TN

38.1: Heavy Ion Performance of a Radiation-Tolerant Flip-Flop Designed for Low-Voltage Applications (3:30)

Grant D. Poe, Marcus S. Evans, Jeffrey S. Kauppila, Timothy D. Haeffner, Lloyd W. Massengill
Reliable MicroSystems LLC, Franklin, TN

Heavy ion testing data is presented on a Radiation Hardened By Design (RHBD) D Flip-Flop (DFF) in a bulk FinFET technology that is designed for reduced vulnerability to radiation induced Single-Event Upsets (SEUs) compared to unhardened commercial DFFs, but with lower area and electrical performance penalties compared to fully single-node hardened DICE DFFs. The DS^2CFF is a DICE-like modification of the Static Single-phased Contention-free Flip-Flop (S^2CFF) that maintains static operation, a single-phased clock, and contention-free transitions that enable robust low-voltage operation. The data shows that the DS^2CFF did not experience SEUs for LETs under 2.40 and showed a 50× to 7× lower SEU cross section compared to an unhardened flip-flop for LETs from 7.27 to 49.29, respectively.

38.2: A Soft Error Tolerant Flip-Flop for eFPGA Configuration Hardening in 22 nm FinFET Process (3:50)

Prashanth Mohan, Siddharth Das, Oguz Atli, Ken Mai
Carnegie Mellon University, Pittsburgh, PA

Joshua Joffrion
Sandia National Laboratories, Albuquerque, NM

We propose a soft error tolerant flip-flop (FF) designs to protect configuration storage cells in standard cell- based embedded FPGA fabrics used in SoC designs. Since the eFPGA configuration storage is static, the master latch of the FF is transparent and unused, except when a configuration is loaded. The proposed dual-storage-mode (DSM) FF reuses the master and slave latches as redundant storage along with a C-element for error correction. The DSM FF was fabricated on a 22 nm FinFET process along with standard D-FF, pulse DICE FF, and TMR FF designs to evaluate SE tolerance. The results of the radiation tests show that the DSM FF can reduce the soft error rate by more than two orders of magnitude (330X) compared to the standard D-FF and an order of magnitude (24X) compared to the pulse DICE FF with comparable area.

38.3: Selective Radiation Hardening for Edge AI Systems: Identifying and Protecting Critical Bits (4:10)

Sanjay Das, Kanad Basu
University of Texas at Dallas, Richardson, TX

Radiation poses significant challenges to the reliability and functionality of hardware systems. While radiation hardening techniques can mitigate these effects, applying them across entire systems is resource-intensive and impractical for edge applications that deploy small models like Binary Neural Networks (BNNs), valued for their low computational and storage demands. A more efficient solution is selective hardening, focusing on critical areas. This paper introduces the Outlier Gradient-based Evolutionary (OGE) framework, a technique that identifies the most vulnerable parameters in BNNs by targeting and flipping critical binary weights. Evaluations on datasets like Fashion-MNIST, CIFAR10, GTSRB, and ImageNet show that altering as few as 150 bits out of 10.3 million can increase misclassification by up to 68.1%, highlighting the potential for selective hardening the critical parameters to protect hardware from radiation-induced faults.

38.4: Inserting SET Filters in Non-Critical Paths (4:30)

Joshua Govan, Phillip Gibson, Daniel B. Limbrick
North Carolina Agricultural and Technical State University, Greensboro, NC

Soft errors mitigation can be costly to performance and circuit size if done across the entire circuit. Several researchers have attempted to selectively mitigate soft errors through filter insertion; however, the selective placement of these filters can potentially affect the overall circuit delay. This paper investigates the feasibility of inserting transient filters into the gaps, and answers: (1) how many filters can be inserted along a path without changing overall circuit delay and (2) how much fault coverage this approach would have. The filter was created using preexisting standard cells. The performance and functionality are verified using static timing analysis and SystemVerilog simulation. Results show that filters can be inserted into non-critical paths without impacting chip delay.

EVENING SOCIAL (OFFSITE) (6:00–10:00)
(Buses begin leaving at 5:00 pm)

SOLID STATE TECHNOLOGY FOR HIGH VOLTAGE PULSED POWER SOURCES

Wednesday, March 19 / 3:30–4:50 pm / Ballroom G

Chair: **Travis Anderson**
University of Florida, Gainesville, FL

Co-Chair: **Zachary Drikas**
U.S. Naval Research Laboratory, Washington, DC

39.1: Si and SiC Closing Switches for High Power Wideband and Ultrawideband Switching **(3:30)**

Jason Sanders
Transient Plasma Systems, Inc., Torrance, CA

Reza Ghandi
General Electric Research, Niskayuna, NY

39.2: Effect of Doping Profile on Silicon Semiconductor Opening Switch **(3:50)**

Caitlin A. Chapin, Qinghui Shao, Dario Labrada, Brent McHale, David Smith, Sara E. Harrison, John Monzon, Matthew Majarucon, Lars F. Voss
Lawrence Livermore National Laboratory, Livermore, CA

Susan Heidger, Brad Hoff, James Schrock
Air Force Research Laboratory, Livermore, CA

39.3: Optimization of Semiconductor Opening Switch Fabrication **(4:10)**

Geoffrey Foster
Jacobs Inc., Washington, DC

Andrew Koehler, Alan Jacobs, Karl Hobart, Joseph Croman, Michael Mastro
U.S. Naval Research Laboratory, Washington, DC

Christopher Wu, Stephanie Wasmuth, Anthony Troxell, Marc Freidson, Soon Chang
Defense Microelectronics Activity, McClellan Park, CA

Michael Hontz
Naval Surface Warfare Center Philadelphia, Philadelphia, PA

Ronald Focia
Envisioneering Inc., Lancaster, PA

39.4: Depth and Substrate Dependence of Heat Dissipation in GaN *p-n* Diodes Bonded to AlN, Diamond, and SiC **(4:30)**

Vincent Meyers, James Loveless, Jeffrey Steinfeldt, Hoang Vuong, Matthew Bahr, Anthony McDonald, Amun Jarzembski, Anthony Rice, Luke Yates, Robert Kaplar
Sandia National Laboratories, Albuquerque, NM

Creation of a metal bond between vertical GaN power devices and more thermally conductive substrates has shown to improve the thermal management of the relatively low thermally conductive GaN. In this work, dissipation of heat from vertical GaN p-n diodes bonded to AlN, SiC, and diamond by a newly developed metal-metal compression process is analyzed. By utilizing complementary steady-state optical thermography techniques, we compare heat dissipation of the device under forward bias near the p-n junction and at the device anode. It is found that while the thermal conductivity of the bonded substrate governs heat dissipation throughout the volume of the bonded diode, the asymmetry of the thermal interface at the front and back side of the diode leads to substantial heating at the top electrode. Implications for thermal management in the context of future device design are discussed.

EVENING SOCIAL (OFFSITE) **(6:00–10:00)**
(Buses begin leaving at 5:00 pm)

THURSDAY, MARCH 20

Breakfast, Ballroom Foyer **(8:00–8:30)**

Session 40 **(TA2 – Emerging Technologies)**

APPLICATIONS OF AI/ML

Thursday, March 20 / 8:20–10:00 am / Ballroom A

Chair: **Manny Trejo**
Department of Defense

Co-Chair: **Brian Hoskins**
Natcast, Washington DC

40.1: Exploring the Use of Time-Series Foundation Models for RF Signal Classification and Interference Quantification (8:20)

Hiroki Mii
Georgia Institute of Technology, Atlanta, GA

Sara Garcia Sanchez, Asaf Tzadok, Wesley M. Gifford, Roman Vaculin
IBM T.J. Watson Research Center, Yorktown Heights, NY

Signal classification and interference quantification are key capabilities for RF situational awareness in critical applications such as network security and anomaly detection. AI inference on raw IQ data can accelerate results in these domains, but deployment is often limited by extensive training. In this context, foundation models (FM) can offer an effective solution, leveraging pretraining on diverse datasets and requiring minimal data for fine tuning. In this exploratory paper, we evaluate a time series FM's performance on RF signal classification and interference quantification. We leverage a FM pre-trained on publicly available forecasting datasets, and enhance its architecture to support classification tasks. We fine-tune the FM using a synthetically generated dataset of signals concurrently containing two waveforms (radar and OFDM) of different power ratios. Our results demonstrate an inference accuracy from 97 to 100% for signal classification and up to 89% for interference quantification.

40.2: Key Requirements for Successfully Implementing Generative AI in Edge Devices – Optimized Mapping to Neural Processing Unit (8:40)

Gordon Cooper, Fergus Casey
Synopsys, Inc., Sunnyvale, CA

In this talk, we explore the emerging trends in generative AI for edge devices and the role of transformer-based neural networks at their core. We investigate the distinct attributes of transformers and how there are advantages over conventional convolutional neural networks (CNNs) enabled Generative AI. The talk discusses key requirements for the latest Neural Processing Units (NPU) to support Transformers and Generative AI constructs to support edge device applications. We use transformer-based vision models, text-to-image, and large language model generative AI examples to illustrate the requirements for efficient mapping onto an NPU.

40.3: An Efficient Convolutional Neural Network Analog Architecture **(9:00)**

Jennifer Hasler, Praveen Raj Ayyappan
Georgia Institute of Technology, Atlanta, GA

This effort presents a first important example of an analog system that requires considerable analog architecture development by developing an architecture for image classification from a typical imager input through a classified result using particular NN algorithm, a Convolutional NN (ConvNN). Given the entire architecture approach, one can evaluate the expected complexities for an analog single IC architecture (1M input, 6 layers) to compute a ConvNN with minimal intermediate storage elements and communication. The architecture is based on image processing algorithms initially developed for FPAA devices and generalized for any analog structure.

40.4: Cross-Correlations and Challenges of Combined Artificial Intelligence, Functional Safety and Cybersecurity Development for Automotive, Aerospace, and Government Applications **(9:20)**

Radu Iacob
Synopsys, Inc., Hillsboro, OR

Shivakumar Chonnad
Synopsys, Inc., Sunnyvale, CA

Chris Clark
Synopsys, Inc., San Antonio, TX

The electric engine and AI-enabled autonomous driving have taken center stage in the automotive industry. From sensor fusion and power optimization to adaptive cruising and robotaxis, development requires cross-correlation of multiple disciplines, including data science, machine learning, and neurocomputing, along with reliability, functional safety, and cybersecurity. The goal is to create solutions for automotive systems that are capable of reliably performing in safety-critical environments while resisting cybersecurity threats. These considerations are also important in the development of aerospace and government solutions. Artificial intelligence is becoming the driving force shaping today's technologies, global economies, the social and cultural environments around the world, hence the need to consider the impact, cross-correlations, and challenges between and within all related disciplines.

40.5: AI-Driven Optimization of Design Parameters for X-Ray Compatibility in Advanced Packaging **(9:40)**

Katayoon Yahyaei, M Shafkat M Khan, Shajib Ghosh, Navid Asadizanjani
University of Florida, Gainesville, FL

Parth Sandeepbhai Shah
Intel Corporation, Phoenix, AZ

The shift towards advanced packaging introduces complex assembly processes that necessitate X-ray imaging for inspection. This transition also presents significant challenges, as the intricate and miniaturized transistors and interconnects in advanced packages lead to critical issues with noise scattering. This paper presents an AI-driven framework designed to integrate X-ray compatibility into the design process by predicting optimal design specifications to enhance imaging quality. The framework combines X-ray noise estimation with Bayesian optimization. A specialized two-stage Bayesian optimization algorithm is employed to minimize computational costs by reducing the number of iterations required to reach an optimal solution. Additionally, the paper proposes a Monte Carlo based simulation method for X-ray imaging noise estimation at the design stage and evaluates the impact of simulation complexity on overall framework performance. Analysis of the framework demonstrate the significance of design optimization in improving yield and highlight its effectiveness in managing the complexities of high-volume manufacturing.

BREAK **(10:00–10:30)**

MINITHERMS3D

Thursday, March 20 / 8:20–10:00 am / Ballroom B

Chair: **Yogendra Joshi**
DARPA MTO, Arlington, VA

Co-Chair: **Aaron Smith**
Booz Allen Hamilton, Arlington, VA

41.1: Cooling Heterogeneously Laminated Integrated Tiers (CooHLIT) (8:20)

Seongchul Jun, Junyoung Lee, Philip Stupar, Keisuke Shinohara, Chris Hillman, Jonathan Hacker, Ganesh Subraminian, Avijit Bhunia
Teledyne Scientific Company, Thousand Oaks, CA

Teledyne Scientific Company (TSC) is developing CooHLIT (Cooling Heterogeneously Laminated Integrated Tiers) – a compact 3D heterogeneously integrated (3DHI) chip stack to air thermal management system under the DARPA Minitherms3D program. CooHLIT incorporates: (1) An interstitial-level silicon (Si) micro-cooler for active liquid cooling of high-power electronics with liquid-to-vapor phase change of a dielectric refrigerant; (2) Integration of the silicon micro-coolers with a tier of functional integrated circuits and 3D stacking with tier-to-tier integration; and (3) A highly efficient, air-cooled condenser system. This technology eliminates the "thermal limitation" of 3D stacking of devices to an arbitrarily large number of layers, enabling unprecedented functionality of micro-electronics components and SWaP (size, weight, and power) improvement at the system level. The near-term targeted application is a tiled power aperture HPM (high power microwave) beam, used as directed energy for powering unmanned vehicles.

41.2: PHased ARray with INnovative HEterogeneously Integrated Thermal Solution (PHARINHEITS) (8:40)

Christopher Roper, John Carlson, Christina Seeholzer, Daniel Kuzmenko, Ignacio Ramos, Avantika Sodhi, Garrett Robertson, Clayton Tu, Junghee Ko, Adam Gross, Dylan Hollrigel, Souren Soukiazian, Dmitry Veksler, Diane Artner
HRL Laboratories, LLC, Malibu, CA

Andres Sarmiento, Tahir Mahmud, Kyle Martin, Felipe Rodrigues de Castro, Michael Ohadi
University of Maryland, College Park, MD

Heungdong Kwon, Haeun Lee, Hyongsoon Lee, Mehdi Asheghi, Ken Goodson
Stanford University, Stanford, CA

Chung-Shuo Lee, Faharia Bhuiyan, Shubhra Bansal, Ganesh Subbarayan
Purdue University, West Lafayette, IN

Chenson Chen, Ryan Keech, Melissa Smith
MIT Lincoln Labs, Lexington, MA

41.3: Si Interposer 2.5D Platform for Thermo-Mechanical Simulation and Reliability Studies in Extreme Environments **(9:00)**

Gabe Velarde, John Holaday, David N. Halbrooks, Darren Crum
Purdue Applied Research Institute, West Lafayette, IN

Josh Atwater, Pete Conway
NHanced Semiconductor, Odon, IN

41.4: Custom Si Chip Fabrication to Benchmark Local Temperatures within 3D Heterogeneously Integrated Stacks **(9:20)**

Ryan Keech, Chenson Chen, Chad Stark, Philip Bailey, Daniel Santiago, Richard D'Onofrio, Tomasz Slanda, Peter Wyatt, Melissa Smith
MIT Lincoln Laboratory, Lexington, MA

John Carlson, Daniel Kuzmenko, Christina Seeholzer, Avantika Sodhi, Ignacio Ramos, Clayton Tu, Dmitry Veksler, Christopher Roper
HRL Laboratories, LLC, Malibu, CA

Innovative thermal management solutions will play a critical role to the implementation and wider adoption of three-dimensionally integrated chip stacks. In order to assess performance of such technologies relevant to the United States Government (USG) and as government furnished capability, Massachusetts Institute of Technology Lincoln Laboratory (MIT LL), has offered access to its Microelectronics Laboratory and other facilities to performers of USG contracts and was included in the HRL Laboratories proposal for DARPA's Minitherms3D program. In this work, MIT LL led the design and fabrication of a custom Si chip for high-power dissipation and local temperature monitoring to benchmark performance of novel cooling technologies in 3-dimensionally integrated chip stacks. The process control schemes and design as well as chip fabrication, performance, and operation are reviewed along with additional potential use cases for this foundational benchmarking technology.

41.5: Three-Dimensional Tiered Heterogeneous EvapoRation-cooled Module (3DTHERM) **(9:40)**

Clayton Pullins
Northrop Grumman Mission Systems, Baltimore, MD

Robert (Bob) Patti
NHanced Semiconductors Inc., Batavia, IL

Craig Zuhlke
University of Nebraska Lincoln, Lincoln, NE

Constantine (Dino) Megaridis
University of Illinois Chicago, Chicago, IL

Rinaldo Miorini
GE Aerospace Research, Niskayuna, NY

BREAK **(10:00–10:30)**

ELGAR

Thursday, March 20 / 8:20–10:00 am / Ballroom C

Chair: **Trish Veeder**
DARPA, Arlington, VA

Co-Chair: **Sharon Woodruff**
Booz Allen Hamilton, Washington, DC

42.1: Improving Accuracy of On-Wafer Calibration and Microelectronic Characterization to Millimeter-Wave Frequencies **(8:20)**

Jerome Cheron
National Institute of Standards and Technology, Boulder, CO
and
University of Colorado Boulder, Boulder, CO

Jeffrey Jargon, Ben Jamroz, Ari Feldman
National Institute of Standards and Technology, Boulder, CO

Rob Jones
National Institute of Standards and Technology, Boulder, CO
and
Colorado School of Mines, Boulder, CO

Antonio Crespo, Paul Watson
Air Force Research Laboratory Sensors Directorate, WPAFB, OH

Michael Elliott, Ryan Gilbert
KBR, Inc., Beavercreek, OH

42.2: A 130 nm InP HBT IC Platform for Future G-band Phased Arrays **(8:40)**

Miguel Urteaga, Zach Griffith, Adam Young, Josh Bergman, Jonathan Hacker, Petra Rowell, Alex Papavasiliou, Mercedes Gomez, Andres Paniagua, Armando Carlos, Logan Whitaker, Dean Regan, Keisuke Shinohara
Teledyne Scientific Company, Thousand Oaks, CA

Matthew Lueck, Krista Morris
Micross Advanced Interconnect Technology AIT, Research Triangle Park, NC

42.3: I-TERA: Low-Power Millimeter Wave and Terahertz Radio Technologies in 16 nm FinFET CMOS **(9:00)**

Farhana Sheikh
Altera, An Intel Company, Portland, OR

Alyosha Molnar
Cornell University, Ithaca, NY

Ali Niknejad, Borivoje Nikolic
University of California, Berkeley, Berkeley, CA

Gabriel Rebeiz
University of California, San Diego, San Diego, CA

Mark Rodwell
University of California, Santa Barbara, Santa Barbara, CA

Xuan Mo, Sirisha Kale, Bryan Casper, Russell Martinelli
Intel Corporation, Hillsboro, OR

Terahertz (THz) (90 GHz to 1000 GHz) communications and sensing ICs are key to enabling next generation wireless systems to address 6G and emerging applications that are delay-sensitive and require very high throughputs, on order of 10 to 100 Gbps. The key question is whether advanced CMOS technologies can provide the required performance for sub-THz applications; and when does it become necessary to move to III-V compound semiconductors to provide the needed gain, linearity, and performance? In this paper, we review 16 nm CMOS sub-terahertz integrated circuits (ICs) developed under DARPA's I-TERA program, leveraging back-end-of-line (BEOL) and front-end-of-line (FEOL) mm-Wave features which include THz wideband transmitters, receivers, clocking circuits, data converters, and N-path circuits at mm-Wave frequencies.

42.4: Progress Towards Planar MMICs and Phased Arrays **(9:20)**

Jeffrey LaRoche, Brian Schultz, Nick Kolias, Clay Long, Eduardo Chumbes, Lovelace Soirez, Jason Milne, Amada Castro, David Crouch, Adam Peczalski, Charles Wang
Raytheon, Tewksbury, MA

Benjamin Powers, Haley Steffen
Collins Aerospace

David Howard
Tower Semiconductor

Robert Patti
NHanced Semiconductors

David Meyer, Virginia Wheeler, Brian Downey
Naval Research Laboratory

Harish Krishnaswamy
Columbia University

Michael Elliott
Air Force Research Laboratory

42.5: ELGAR: Creating High-Density Interconnects and Integration for Non-Silicon Devices **(9:40)**

Trish Veeder, Iskren Abdomerovic
DARPA, Arlington, VA

Sharon Woodruff
Booz Allen Hamilton, McLean, VA

BREAK **(10:00–10:30)**

MULTIDISCIPLINARY APPROACHES TO SECURITY

Thursday, March 20 / 8:20–10:00 am / Ballroom D&E

Chair: **Jonathan Cruz**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Gio Kao**
Sandia National Laboratories, Albuquerque, NM

43.1: Structured Assurance Cases for Microelectronics: Overview and Automation (8:20)

Jeremy Bellay, Christopher Taylor, Eric Bauer, Max Chambers, Adam Kimura
Battelle Memorial Institute, Columbus, OH

Assurance for microelectronics has been attempted through various means throughout the years from certifications through trusted foundries model to hybrid data-driven checklist approach via quantifiable assurance. In this work, we review the structure and use of structured assurance cases across a range of industries. We describe an AI powered automated system for the collection of evidence that supports and disputes a user provided claim, reducing both the effort required for assurance case development and the potential for confirmation bias. Finally, we discuss how assurances can be implemented for the micro-electronics supply chain and improve upon the current check list method while retaining rigor. The assurance case approach represents a significant paradigm shift in how to conduct the assurance of microelectronics. This shift necessitates a comprehensive understanding and meticulous application of assurance case methodologies.

43.2: Cryptographic Protocols for Trusted & Untrusted Chiplet Interaction (8:40)

Olsan Ozbay, Daniel Xing, Ankur Srivastava
University of Maryland, College Park, MD

Dana Dachman-Soled
Institute for Systems Research, University of Maryland, College Park, MD

As the demand for higher performance grows, and traditional Integrated Circuits (ICs) struggle to get smaller in terms of form factors, 3D Integrated Circuits (3D ICs) have emerged as a promising solution due to their ability to stack multiple layers of circuits vertically, significantly enhancing performance and size. However, these 3D ICs have different fabrication processes and supply chain vulnerabilities, which lead to some layers not being trusted, and further security risks. To mitigate these risks, this paper proposes a novel approach inspired by private information retrieval (PIR) schemes, leveraging replicated databases, and using multiple adders simultaneously to protect data within the untrusted layers of 3D ICs during mathematical operations. This approach aims to provide a cost and time effective solution to the security challenges in 3D ICs, when a data flow graph (DFG) consisting of said mathematical operations needs to be computed fully or partially on these untrusted layers.

43.3: A Methodology for Trusted Integrated Circuits via Asynchronous Design and Split Manufacturing (9:00)

Tristan J. Hudson, Anvesh K. Perumalla, John M. Emmert
University of Cincinnati, Cincinnati, OH

Integrated circuits are becoming increasingly vulnerable to side-channel attacks, which exploit physical properties like power consumption and electromagnetic radiation to extract sensitive information. These attacks pose a significant threat to critical national assets. A promising defense is clockless asynchronous design, which reduces power consumption, lowers electromagnetic emissions, and spreads computation over time, reducing vulnerabilities to attacks. However, typical asynchronous designs tend to be 1.5× to 2× larger than synchronous designs, posing implementation challenges. Maskconfigurable circuits, combined with split manufacturing, offer an additional security layer. In split manufacturing, the lower layers — such as polysilicon and diffusion — are fabricated at an untrusted, low-cost foundry, while the higher metal layers are completed later at a trusted foundry. This paper presents an asynchronous design flow using split manufacturing and a novel hybrid methodology to tackle the usual area increase, achieving secure designs with only a 7% area overhead.

43.4: Anomaly Detection Methodology for Zero-Trust Architecture-Based Systems-on-Chip (9:20)

Abigail Butka, Peter Forcha, Antonio Hendricks, Christophe Bobda
University of Florida, Gainesville, FL

Zero-Trust Architectures (ZTA), proposed by the National Institute of Standards and Technology (NIST), improve security through a strict 'never trust, always verify' ideology. As embedded systems are increasingly powered by Systems-on-Chip (SoC), their exposure to malicious third-party components and attacks increases. Extending ZTA to SoC enhances security by reducing SoC's attack surface and adding real-time monitoring of all system transactions to enforce user access based on trust. This paper presents, to our knowledge, the first autoencoder (AE) implemented in hardware to address the lack of system logging and monitoring solutions for ZTAs implemented on SoC. Preliminary findings demonstrate the AE's accuracy in identifying anomalous transactions across three testcases, with one dataset producing an error approximately 7,139× larger than non-anomalous datasets. The final version of this paper will expand upon these results by providing an assessment of the AE's performance, resource utilization, and its effectiveness in real-time monitoring.

43.5: FPGA Safety and Security Policy Compliance via HDL-to-Bitstream Equivalence Checking (9:40)

Jonathan Graf, Margaret Winslow, Evan Drinkert
Graf Research Corporation, Blacksburg, VA

Kevin Urish, John Hallman
Siemens EDA, Wilsonville, OR

Security and safety policies across domains such as embedded security, defense safety, and automotive safety have been updated to require the ability to prove the design in an FPGA bitstream matches the anticipated function and structure specified in a designer's source. Until recently, there were no commercial tools to meet these requirements. Now, emerging tools for bitstream equivalence checking can be paired with established tools for logic equivalence checking to create a verification chain that satisfies these new policy demands. This paper explores three example safety and security policies. A demonstration design is evaluated with logic and bitstream equivalence checking tools, and the output files necessary to seamlessly link the conclusions of each tool as required by policy are enumerated. Finally, additional assurance requirements that can be met by pairing bitstream equivalence checking tools with other verification techniques are explored.

BREAK (10:00–10:30)

NEW MATERIALS FOR HIGH PERFORMANCE MICROSYSTEMS

Thursday, March 20 / 8:20–10:00 am / Ballroom H

Chair: **Zachary Fishman**
Booz Allen Hamilton, Washington DC

Co-Chair: **Dmitry Ruzmetov**
US Army Research Laboratory, Adelphi, MD

44.1: SmartCut Alternative for Thin-Film Lithium Niobate Production (8:20)

Anna Braun, Xiaohui Wang
SRI International, Princeton, NJ

Nicole Heidel
SRI International, Boston, MA

44.2: Engineering Ferromagnetic Resonance in Thin Film YIG via Ion-Implantation Technique (8:40)

Henri Baldino, Daniel Hedlund, Piotr Kulik
University of Central Florida, Orlando, FL

Dmytro Bozhko
University of Colorado Springs, Colorado Springs, CO

We have investigated the properties of Al implantation in a thin film stack consisting of YIG/GGG/YIG using a low, 10^{13} cm^{-2} (Y2), and a high, 10^{15} cm^{-2} (Y6), ion fluency. Specifically, the static and dynamic magnetic properties have been investigated. Our findings indicate that a higher ion fluency gives a larger reduction of magnetic saturation, and thus a shift to lower ferromagnetic resonance frequencies. Additionally, since only one side of the YIG is implanted, one-sided changes are seen when measuring the ferromagnetic resonance of the samples. Furthermore, the static magnetic properties hint at a local shift in magnetic anisotropy. These changes in material properties could translate to a post-modification alteration of the material thus enabling new devices.

44.3: PEALD of Ga_2O_3, Al(O,N), GaN for RF Devices (9:00)

Joseph Casamento, Dadam Kang, Loïs Talli, John Niroula, Tomás Palacios
Massachusetts Institute of Technology, Cambridge, MA

This report details plasma enhanced atomic layer deposition (PEALD) of ultrawide bandgap Ga_2O_3, Al(O,N), and GaN at temperatures of 250 °C. Ga_2O_3 and Al(O,N) less than 19 nm thick on W/Si layers display large breakdown fields in excess of 6 MV/cm. Highly crystalline GaN can be achieved at less than 15 nm thickness on c-plane sapphire substrates. This work presents progress toward the utilization of PEALD for deposition of ultrawide bandgap semiconductors as passivation layers for radiofrequency (RF) devices.

44.4: 3DHI Wafer Level Manufacturing Advances at RTX – Raytheon Vision Systems **(9:20)**

Eric Miller, Sean Kilcoyne, Jason Milne, Aaron George, Amanda Rickman, George Grama, Christine Frandsen, Jon Sigurdson, Alphonse Kamato, Kevin Meneou
Raytheon, Lompoc, CA, El Segundo, CA and Dallas, TX

44.5: Maturing Co-Packaged Optics Technology towards Prototype & Technology Transition **(9:40)**

Kumar Abhishek Singh, Ziyin Lin, Peter A Williams, Darren A Vance, Joel Wright, Bilas Chowdhury, Todd R Coons, Shahin Mani, John Christopher Decker, Matthew Fritz, Vamsi Chandra Meesala, Pratyasha Mohapatra, Shivani Syal, John Oh, Saikumar Jayaraman
Intel Corporation, Santa Clara, CA

BREAK **(10:00–10:30)**

RADIATION HARD CHARACTERIZATION MECHANISMS

Thursday, March 20 / 8:20–10:00 am / Ballroom G

Chair: **Jeffrey Teng**
The Aerospace Corporation, Chantilly, VA

Co-Chair: **Patrick Nsengiyumva**
The Boeing Company, Huntington Beach, CA

45.1: Impact of N-Implantated Termination on Single Event Effects (SEEs) in Vertical GaN Power Devices **(8:20)**

Andrew Koehler, Ani Khachatrian, Alan Jacobs, Cory Cress, Karl Hobart, Michael Mastro
U.S. Naval Research Laboratory, Washington, DC

Geoffrey Foster
Jacobs, Inc., Washington, DC

Tolen Nelson, Raghav Khanna, Daniel Geogiev
University of Toledo, Toledo, OH

45.2: Evaluating the Radiation-Hardness of Varying COTS EEPROMs in a Thermal Neutron Environment **(8:45)**

Riley Madden, Stylianos Chatzidakis, Peter Bermel, Fraser Dougall, Brian Dodd, Hannah Pike
Purdue University, West Lafayette, IN

Electronically erasable programmable read-only memories (EEPROMs) are used commonly on spacecraft, and thus are exposed to high levels of ionizing radiation, including thermal neutrons. Determining commercial off the shelf (COTS) EEPROM devices' resilience in these environments increases the reliability of these spacecraft systems. This research studied the effects of a thermal neutron environment on the degradation of COTS EEPROMs using a Subcritical Assembly to expose the devices to a thermal neutron flux. The failure rate of the EEPROM devices controlled by time and neutron flux were studied. First, the spatial distribution of neutron flux within the Subcritical Assembly was determined via Neutron Activation Analysis. Then, using this information, several EEPROMs were tested at once. This experiment design allowed for observation of varying degradation between different memory capacities, package types, neutron fluxes, and irradiation times.

45.3: Flux-Dependent Strategic Neutron Effects: A Summary of Recent and Ongoing Research **(9:10)**

Joshua Joffrion, Nathaniel Dodds, Nathan Nowlin
Sandia National Laboratories, Albuquerque, NM

45.4: Machine Learning Based Prediction of Neutron-induced Failure Time of 1200 V and 1700 V SiC Power Devices **(9:35)**

Christopher Stankus, Moinuddin Ahmed
Argonne National Laboratory, Lemont, IL

Stephen Arthur Wender, Kranti Gunthoti
Los Alamos National Laboratory, Los Alamos, NM

This work is focused on the development of a predictive model for the reliability of wideband gap (WBG) SiC power transistors exposed to terrestrial neutron radiation using machine learning techniques. Wide bandgap SiC power transistors are attractive candidate for aerospace and satellite communication which offer smaller footprint, lower weight, higher-temperature operation, lower power losses, and higher operating frequency. Machine learning enables the discovery of predictive signals for neutron reliability from device characteristics. We have developed a machine learning model which can predict the failure of devices and provide a predicted neutron fluence at which failure occurs. The model we have developed uses gradient-boosted trees for predicting device failure and for assigning a neutron fluence. Trained and tested in this way the model has an accuracy of 95% when classifying failures.

BREAK **(10:00–10:30)**

POSTER SESSION

Thursday, March, 20, 2025/ 10:30 am–12:00 pm / Exhibit Hall

Advanced Materials and Processes Posters

(TA1 – Advanced Materials and Processes)

P.1: Optimal Precursor Dosing Condition for ALD Deposited TiN with Titanium Tetrachloride and Hydrazine

Amy E. Ross, Dipayan Pal, Ping Che Lee, Diego Mora, Jannick Fammels, Dohyun Go, Andrew Kummel
University of California, San Diego, La Jolla, CA

Danish Baig, Muhannad S. Bakir
Georgia Tech School of Electrical and Computer Engineering, Atlanta, GA

Jeffery Spiegelman
RASIRC, Inc., San Diego, CA

With the rise of AI integration in commercial and defense application, the demand for high bandwidth memory (HBM) has grown which pushed the limits of 2D technology to 3D architectures. Precise control over deposition processes is critical for achieving conformal coatings in high aspect ratio 3D structures. Atomic layer deposition (ALD) has become essential for ensuring uniformity at the nanoscale. This study identifies the optimal saturation doses for TiN ALD which is a diffusion barrier necessary for horizontal vias in DRAM. Titanium tetrachloride ($TiCl_4$) and hydrazine (N_2H_4) as precursors were utilized to make conformal, conductive films. At 475 °C, $TiCl_4$ required a 300 ms pulse, while N_2H_4 needed 2750 ms. This stark contrast in pulse lengths is addressed through a theoretical model enabling conformal processing of horizontal vias for HBM and other 3D structures in c-FET critical for energy efficient AI technology.

P.2: Electroless Copper Deposition of Laser-Induced Graphene for Advancing Flexible Hybrid Electronics

Attila Rektor, Josh Eixenberger, Tony Varghese, Brian Cummings, Michael Curtis
Boise State University, Boise, ID

P.4: Additive Manufacturing of Silicon Nitride (Si_3N_4) Radomes with High Mechanical Properties

Xiaoling Shi, Hui Lu
Winchester Technologies, LLC, Burlington, MA

Yuhui Xiang, Dong Lin
Oregon State University, Corvallis, OR

Bin Luo, Steven Zhang, Shengli Zhang, Nian X. Sun
Northeastern University, Boston, MA

Guang Yang, Narges Malmir, Shuting Lei
Kansas State University, Manhattan, KS

Chenyang Zhu, Xin Zhao
Clemson University, Clemson, SC

Mohan Sanghadasa
US Army DEVCOM Aviation & Missile Center, Redstone Arsenal, AL

In the field of aerospace technology, the demand for materials capable of withstanding the extreme conditions of hypersonic flight is ever-growing. Hypersonic vehicles, surpassing Mach 5 speeds, necessitate advancements in materials science. Silicon nitride (Si_3N_4) stands out as the material of

choice for hypersonic radomes due to its exceptional thermal stability, thermal shock resistance, and mechanical strength. However, traditional manufacturing methods for Si_3N4 radomes pose limitations in terms of time, cost, and design flexibility. Additive Manufacturing, commonly known as 3D Printing, offers an innovative solution. This paper explores the application of Additive Manufacturing to Si_3N4 radome production. Additionally, this paper did a systematic study of CNC binder contents on the mechanical properties of printed silicon nitride ceramics. So far, our printed Si_3N4 cylindrical samples showed high hardness with 23 GPa and high flexural strength with 90.75 MPa.

P.5: Synthetic Diamond Production via Pyrolysis of Poly(naphthalene-co-hydridocarbyne)

Dane Arthur James Williams Miller,
Francis Patrick McCluskey
University of Maryland, College Park, MD

Roger Brewer, David Findley
Lockheed Martin Corporation, Dallas, TX

As transistors approach atomic scales, new strategies are needed to enhance the speed and efficiency of semiconductor devices beyond merely increasing transistor density. While higher density improves computing power, it also raises volumetric energy density, requiring innovative heat dissipation methods. One promising approach involves using synthetic diamond substrates instead of silicon, as diamond's thermal conductivity can be up to 1200% higher than that of silicon, depending on quality and temperature. Additionally, diamond's larger band gap (5.47 eV) compared to silicon (1.12 eV) may enable more reliable performance at elevated temperatures. Traditionally, synthetic diamond has been produced through chemical vapor deposition (CVD), but a simpler and more cost-effective method using pyrolysis of solid-state polycarbynes could reduce the need for extensive post-processing of diamond films.

P.6: Band Alignment Analysis of ε-$(In_xGa_{1-x})_2O_3$/AlN Interface via X-ray Photoelectron Spectroscopy

Maria Sultana, Ariful Haque
Texas State University, San Marcos, TX

Ultrawide bandgap (UWBG) oxide-nitride heterojunctions have become increasingly critical for next-generation microelectronic devices due to their ability to combine the advantages of high breakdown fields, bandgap tunability and excellent thermal properties, all essential for high-power and high-frequency applications. This study focuses on investigating the growth and band alignment study of UWBG ε-$(In_xGa_{1-x})_2O_3$/AlN heterojunction to address both electronic and thermal challenges in advanced devices. By employing pulsed laser deposition (PLD), phase-pure ε-$(In_xGa_{1-x})_2O_3$ thin film was successfully grown on AlN/sapphire substrates. PLD growth optimization experiments revealed that achieving the metastable ε-$(In_xGa_{1-x})_2O_3$ phase requires moderate deposition temperatures, high oxygen pressure, and elevated laser energy density. Band alignment analysis using XPS-based Kraut's method revealed a significant conduction band offset of 1.7 eV, providing a strong barrier against electron leakage, while the obtained valence band offset is 0.03 eV. These findings pave the way for advancing UWBG-based high-power devices, UV photodetectors, and future communication technologies.

P.7: Time Critical Ethernet – The Future of Aerospace

Chinh Le
LeWiz Communications, Inc., Sunnyvale, CA

Time Triggered Ethernet (TTE) and Time Sensitive Network (TSN) are 2 standards defined by SAE and IEEE for future networking which support deterministic, real time and mixed traffics. TTE has been used in aviation and space. TSN is fairly recent. Applications for aerospace require high integrity, high reliability, fault tolerant. Space vehicles, hypersonic systems further require radiation hardened electronics supporting these standards. This paper discusses the 2 standards, its current states, how it may co-exist with older aerospace network technologies such as Mil 1553, Mil 1394, etc. It will also present rad-hard electronics supporting TTE and TSN for government applications

P.8: Leveraging Machine Learning Force Fields (MLFFs) to Simulate Large Atomisitic Systems for Fidelity Improvement of Superconducting Qubits and Sensors

Søren Smidstrup, Shela Aboud, Ricardo Borges, Anders Blom, Pankaj Aggarwal, Robert Freeman, Jamil Kawa
Synopsys, Inc., Sunnyvale, CA

Quantum Computing Superconducting qubits and Superconducting sensors are Two-Level Systems (TLS) modeled in a double well potential. Traditional bulk Density-Functional Theory (DFT) methods do not adequately capture the complete physics including key aspects and dynamics of superconductivity. Superconductivity at the atomistic level is inherently modeling quantum-mechanical properties, but complexity limits modeling at scale. In this paper we will describe the challenges of modeling and the simulation methods to describe the band structure of topological insulators and non-equilibrium Green function (NEGF) to compute the characteristics of interfaces for superconductivity, along with topological, and thermal properties. The QuantumATK tool leverages density functional theory (DFT) with plane wave LCAO basis sets, semi-empirical methods, conventional Force Fields (FFs) and Machine Learning FFs (ML FFs). In this paper we study the SIS junction to improve sensitivity, coherence and lifetime, of qubits and sensors, leveraging MLFFs to simulate 100,000 atom systems.

P.9: Improving Productivity with Parallel Simulation

Jonathan Stanley
Siemens, Peoria, AZ

Preston McOmber
Moog, Gilbert, AZ

Shuying Qi
Siemens, Fremont, CA

P.10: High-sensitivity Operation of an RF Optically Pumped Magnetometer in Earth's Field

Jonathan E. Bainbridge (Dhombridge), Peter D. D. Schwindt
Sandia National Laboratories, Albuquerque, NM
and
University of New Mexico, Albuquerque, NM

Jeffrey Bach, Neil R. Claussen
Sandia National Laboratories, Albuquerque, NM

P.113: Case Study: A Small Business's Journey in Domesticating Semiconductor Equipment

Lex Keen
SecureFoundry Inc., Fort Worth, TX

The story of how SecureFoundry, a service disabled veteran owned small business took ownership of the most promising Multi-Electron Beam Direct Write (MEBDW) Lithography system on the planet, successfully domesticated it to the U.S., safeguarded it from foreign competitors, and ensured its continued development rather than being shelved by industry giants.

Poster Session

(TA4 – High Performance Digital and Mixed-signal Technologies)

High Performance Digital and Mixed-Signal Technologies Posters

P.11: A 4.3 GHz Digital-Sampling PLL with Noise-Shaping SAR ADC Phase Detector

Matthew R. Belz, Zhengqi Xu, Hsiang-Wen Chen, Seungheun Song, Michael P. Flynn
University of Michigan, Ann Arbor, MI

A digital-sampling PLL based on a noise-shaping SAR (NS-SAR) analog-to-digital converter (ADC) breaks the quantization noise limitation of prior ADC based PDs and enables a lower resolution ADC quantizer and CDAC to be used. Additionally, this improved ADC resolution reduces the PD gain requirement and improves the lock performance. The 2nd-order noise-shaping of the NS-SAR ADC improves the PD resolution and reduces the in-band quantization noise. ADC input-referred noise (e.g. comparator noise) is also reduced in band. Measurements verify that noise shaping reduces the in-band noise by around 7 dB. The CMOS prototype fabricated in a 28 nm process operates at 4.3 GHz and consumes 13.7 mW. The measured RMS integrated jitter from 1 kHz to 100 MHz is 133 fs.

P.12: High Rate Matrix Transpose Operations Using HBM FPGA

Michael Parker
Raytheon Company, El Segundo, CA

Michael Cervantes
Raytheon Company, Tewksbury, MA

Ben Plotner
Raytheon Company, Hanover, MD

Matrix transpose operations (sometime called corner turns) are used in many applications, such as neural network processing, pulse-Doppler processing, back projection algorithm and more. With the introduction of High Bandwidth Memory (HBM) integrated into Field Programmable Gate Array (FPGA) devices, extreme high-rate matrix transpose operations can be achieved. The implementation of large matrix transpose operations using HBM is non-trivial, and involves many design optimizations during the development to achieve high bandwidth across all the HBM channels. This paper will present an approach for achieving very high-rate matrix transpose operations to support multiple channels with a sampling rate of 2.0 complex GSPS for a matrix size of 16384 × 16384 complex samples, not previously achieved in the documented literature. This approach can be further scaled to support matrix transpose operations of a single channel of a billion or more complex samples.

P.13: Automated MATLAB-to-HLS Conversion and Exploration for DoD ASIC/FPGA Development

Michael Parker
Raytheon Technologies, El Segundo, CA

Kirk Ober, Michael Bruennert
Cadence Design Systems, San Jose, CA

While relatively new when compared to more traditional RTL design entry methods, high-level synthesis (HLS) now has two decades of successful tapeouts. However, its use with MATLAB was a manual process. Many HLS designs begin as MATLAB models which must first be rewritten by hand in SystemC before they can be turned into hardware. This paper recounts our experience using a new automated flow available in MATLAB's HDL Coder app. With this flow, we automatically converted our MATLAB M-code files into SystemC modules and ran them through the Cadence Stratus HLS synthesis tool. We also used Cadence Cerebrus, a machine learning tool that works with Stratus HLS, to define an exploration space and let it find the gate-level result with the very best area and power. With this approach, we ultimately exceeded the PPA results for an earlier handwritten, manually explored SystemC version of the same design.

P.14: Advances in Mixed Signal SoC Design Validation Using Simulators and Emulators

Rajat (Raj) Mitra
Cadence Design Systems Inc., Burlington, MA

Eric Juergensen
Cadence Design Systems Inc., Columbia, MD

Traditional SoC (System on Chip) that were predominantly built off of logic gates and rapidly incorporating complex analog functionality. This posed significant challenges to verify and validate their functionality during design. This paper details novel simulation and emulation methodologies to increase design confidence when building such mixed signal (analog and digital) integrated circuits.

P.15: Cold CMOS SRAM Design Opportunities

Rouwaida Kanj
Synopsys Inc., Austin, TX

Jamil Kawa
Synopsys Inc., Mountain View, CA

With the MOSFET characteristics improving dramatically at cryogenic temperatures, a plethora of design opportunities arise. In this work, we propose a novel 5T Half-SRAM design for cold CMOS physical unclonable function (PUF) applications. The 5T cell is area efficient and data remanence-aware and offers a versatile solution to SRAM type memories. The design builds on the low leakage characteristics of cold CMOS and eliminates the need for voltage ramp-up and power-on/off cycles thereby evading pre- and post-erasure PUF attacks. We also propose bleeder designs for handling data remanence issues in traditional SRAM design solutions. The bleeder designs can be used jointly or independently and activate automatically without the need for external triggers thereby guarding against cold boot attacks.

P.16: Low Power Capacitor Sensor Array

Krishna Shivaram, Mark Anthony Santoro, Phung Phan, Bronson Edralin, Rodrigo Cuba
Raytheon Technologies, El Segundo, CA

P.17: Runtime Precision-Reconfigurable AI Accelerator Design

Rouwaida Kanj
Synopsys Inc., Austin, TX

Jinane Bazzi, Ahmed Eltawil
KAUST, Thuwal, Saudi Arabia

Mohammed Fouda
Rain Neuromorphics, San Francisco, CA

The vast number of required multiply and accumulate (MAC) operations for artificial intelligence (AI) applications poses a challenge to traditional Von Neumann architectures. Compute-in-memory (CIM) architectures have been proposed for accelerating MAC operations. There is a rising demand for flexible architectures that balance the model accuracy requirements and design performance efficiency. In this work, we propose a re-configurable analog static random-access memory (SRAM)-based analog IMC macro design that supports 2, 3, and 4-bit precision for each of the input, weight, and output. We assess the design based on a 64 × 180 SRAM-CIM macro. Our macro achieves a normalized peak throughput of 13.8 TOPS, a normalized peak energy, and area efficiencies of 292 TOPS/W, and 166 TOPS/mm^2 respectively.

P.18: CryoPDK: A Cryogenic Temperature Digital Design Flow

Ali H. Hassan, Julia Bi, Puneet Gupta, Sudhakar Pamarti, Chih-Kong Ken Yang
University of California, Los Angeles, Los Angeles, CA

Cryogenic computing has the potential of achieving substantial energy-efficiency by making small adjustments to an existing technology node's devices. This paper introduces a technology retargeting approach to develop a cryogenic design kit (CryoPDK) based on a 14-nm FinFET technology calibrated with hardware data. A multi-supply library is characterized at optimized supply and threshold voltages based on device and interconnect characteristics at the target 77 K. The CryoPDK is applied the RTLs of processor cores to explore logic performance. A processor core framework implemented with the CryoPDK achieves over 20× power reduction compared to conventional technologies operating at room temperature. The design flow incorporates dynamic supplies and introduces selectable supplies for critical path elements to reduce sensitivity to threshold variation on performance.

P.19: Explainable Probabilistic Models on Coarse-Grained Reconfigurable Architectures

Md Tanvir Arafin, Yanze Wu, Shou Matsumoto, Paulo Costa
George Mason University, Fairfax, VA

Recent hardware accelerators and algorithm design innovations have delivered powerful computational capabilities at the edge. Although there has been significant progress in neural network-based artificial intelligence, a marked research gap exists in leveraging these new generations of accelerators for explainable probabilistic models and systems. Thus, we are facing a hardware lottery where domain-specific hardware and computing for complex learning solutions will deliver the new generation of robust and explainable intelligence. This work demonstrates the promises of emerging coarse-grained reconfigurable architectures in accelerating explainable probabilistic models.

P.20: Linearity Enhancement in Segmented, Current-steering DACs Using Modified Switching

Jeffrey S. Walling, Behdad Jamadi
Virginia Tech, Blacksburg, VA

This paper proposes a modification to the switching used in segmented current-steering digital-to-analog converters (CS-DACs) which is applied to a proposed sub-DAC. The proposed techniques not only allow for reduced die area, but also reduce power consumption while the static non-linearity can be kept similar to the conventional segmented CS-DACs. The MATLAB model of the proposed DAC is tested for the performance of the DAC under ideal and non-ideal cases. A prototype in 22 nm FDX-SOI is demonstrated.

P.21: Autonomous Drones in Extreme Conditions

Christophe Bobda, Wade Fortney
University of Florida, Gainesville, FL

P.22: A New Design Space Optimization Flow for COLD / CRYO CMOS & FD-SOI

Jamil Kawa, Stephen Whiteley, Robert Freeman
Synopsys, Inc., Sunnyvale, CA

A STCO/DTCO design flow for COLD CMOS that adds the variable of cooling costs to the PPA design space. It also uses AI/ML for optimizing VDD, temp of operation and cooling costs to achieve PPA targets

P.23: Reasoning-Guided AI for Robust Near-Sensor Processing

Hanning Chen, Wenjun Huang, Yang Ni, Mohsen Imani
University of California Irvine, Irvine, CA

P.24: Breaking the Barrier to X-Band Every Element Digital Beamforming

Peter Delos, Sam Ringwood
Analog Devices, Inc., Durham, NC

Digital Beamforming phased array developments are continually progressing toward an every element digital implementation for improved antenna pattern programmability and multi-mission platform objectives. Every element digital phased arrays exist at S band where element spacing can accommodate the electronics. X-Band is the next frontier for every element digital beamforming implementations. To achieve this level of integration, continued improvement in RF electronics, particularly RF data converters is needed to provide multi-channel, direct sampling, low power direct sampling data converter offerings for implementation in larger phased arrays. In this paper we summarize an 8T8R transmit/receive application based on a data converter IC capable of direct receiver sampling and transmit waveform generation in a 2 GHz bandwidth at X-Band.

P.25: Neuromorphic Digital-Twin-based Control for Multi-UAV System Deployment

Reza Ahmadvand, Sarah Safura Sharif, Yaser Mike Banad
University of Oklahoma, Norman, OK

This study proposes a neuromorphic digital twin (DT) architecture to improve energy efficiency and situational awareness in multi-UAV systems. Combining cloud and edge computing, the architecture features (1) a cloud-based controller for collision-free formation tracking and distributed obstacle avoidance inspired by the behaviors of tilapia fish and pigeons and (2) spiking neural network (SNN) controllers on edge devices trained via supervised learning. This approach enhances energy efficiency, reduces cloud-edge communication, and adapts to environmental changes. Modeling and simulations validate the architecture's effectiveness in complex trajectory-tracking scenarios, offering a robust solution for UAV network control in civil applications.

P.27: Accelerating 3DIC Designs for Aerospace and Government Applications with UCIe IP

Scott Knowlton, Aparna Tarde, Sajani Patel
Synopsys, Inc., Sunnyvale, CA

UCIe enables efficient interoperability between heterogeneous dies (chiplets) in a single package, while optimizing for power, performance, and latency. The latest spec version 2.0 builds on these capabilities with support for more advanced packaging, customized chiplet selection, manageability system architecture, higher bandwidth density and improved power efficiencies. The industry's rapid adoption of UCIe for robust die-to-die connectivity is seen for a wide range of highly customized low volume applications in high-performance computing and automotive, with important implications for government and defense applications. This paper will delve into the UCIe IP variants for standard and advanced packaging and how government and DIB designers can make performance and cost tradeoffs. We will present an application of high-bandwidth UCIe IP for AI Data Center design with a 40 Gbps transmission rate, while maintaining compliance with the UCIe specification.

P.28: Optimizing PPA Benefits from Intel 18A Using Fusion Compiler

Andy Inness
Synopsys, Inc., Austin, TX

Ashish Khurana
Synopsys, Inc., Sunnyvale, CA

Jared Anderson
Synopsys, Inc., Montbonnot, France

As the semiconductor industry continually strives to meet the needs of Moore's law, not only will the Silicon process and manufacturing need to improve, but the Electronic Design Automation (EDA) industry must enhance their tools and methodologies so designers can take advantage of the improvements. The introduction of the Gate-All-Around (GAA) transistor and the PowerVIA architecture in Intel's 18A process represent the next major advancements in semiconductor technology. Intel Foundry and Synopsys collaborated to add new cutting-edge EDA tool technologies to Synopsys' Fusion compiler to maximize these advancements across a wide range of design styles and priorities.

P.29: Best Practices on Utilizing State-of-the-Art (SOTA) Technologies to Meet the Defense Industry's Strict Size, Weight, Power, and Cost (SWaP-C) Requirements

Stephanie Pusch
Trusted Semiconductor Solutions, Brooklyn Park, MN

Ajay Sharma
Intel Foundry, Santa Clara, CA

David Doan
Intel Foundry, Los Gatos, CA

Trusted Semiconductor Solutions (TSS) and Intel Foundry collaborate to ensure DIB applications are supported with end-to-end (E2E) solutions, tailored to meet the critical demands of national security and defense. TSS plays a pivotal role in Intel Foundry's USMAG alliance, helping DIB customers transition to the Intel 18A node and successfully achieve their design goals. TSS develops custom design flows and IP to support IC development on the Intel 18A process node. TSS's has a comprehensive approach to onboard customers, streamline the design process, and ensure mission success through design preparation that enables the novel technology innovations in the Intel 18A node, namely leveraging the PowerVia to fully utilize the benefits of the Back Side Power Delivery Network (BSPDN) and nuances of the RibbonFET technology, and sharing best-known methods for optimizing designs. Benchmarks and key insights from TSS' collaboration with Intel Foundry illustrate how customers can fully leverage Intel's SOTA technologies.

P.30: Features and Applications of Floating Point FPGAs

Michael Parker
RTX Corporation, El Segundo, CA

Jody Forland
Intel PSG, San Jose, CA

Former generations of FPGA devices were optimized for fixed-point operation, and significant penalties in resource utilization, power consumption, and processing bandwidth have been associated with using them for floating-point implementations. FPGA suppliers have recently changed this paradigm by including hardened floating point DSP blocks in their devices and expanding support tools to ease the burden of implementing floating point algorithms. The result is a massive increase in the floating-point capability of FPGAs, with performance of up to 40 Teraflops theoretically possible in the latest devices. Understanding the possibilities created by this new capability is important for engineers working in DSP and it is critical to enabling widescale use of the technology in large designs. This paper details the state of the art in floating point FPGA hardware and support tools. Applications where floating point FPGAs represent a critical advantage are presented with simulation and build results to demonstrate achievable performance.

P.32: Accelerating Intel 18A with the Synopsys Fusion Design Platform

David Gradin, Terence O'Brien, Sovan Kumbhakar
Synopsys, Inc., Sunnyvale, CA

The Defense Industrial Base (DIB) is aggressively seeking greater access to state of the art (SOTA) technology that can be fabricated in the USA. The Intel 18A process is being deployed on the RAMP-C program and is being considered for other advanced System on Chip (SoC) designs. Synopsys and Intel Foundry have been collaborating closely to successfully deploy new software technology for designing with the Intel 18A process. This collaboration allows experts from both sides to identify and address the challenges with an emphasis on packaging solutions with broad leverage. The solution combines product Reference Methodology (RM) scripts with a matched Intel Foundry Process Design Kit (PDK) plugin. It includes support for the entire RTL-to-GDSII flow using the Synopsys Fusion Design Platform. The Synopsys solutions have now been successfully proven at several key U.S. government customers.

HOTS Posters

(TA5 – Packaging, Integration, Thermal and Control Technologies)

P.33: High-Temperature Characterization of Deep Recessed N-Polar GaN HEMT

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N-Polar GaN HEMTs have superior performance than their Ga Polar counterpart in W-band as they can get better 2DEG confinement, ohmic contact, scalability, and pinch-off characteristics. To understand the limits of N-Polar HEMTs for high-temperature applications, a series of measurements were taken at various temperatures above room temperature (25 °C). Through DC-IV measurements at temperatures of up to 300 °C (573 K), Ron and Ion/Ioff ratio were observed, showing the robustness of the HEMTs.

P.34: Bi-Layer Lithium Niobate Diaphragms for High Temperature Pressure Transducers

Xiaoyu Niu, Zihuan Liu, Vakhtang Chulukhadze, Yinan Wang, Ruochen Lu, Neal Hall
University of Texas at Austin, Austin, TX

Lezli Matteo, Nishanth Ravi, Eugene Kwon, Mark S. Goorsky
University of California, Los Angeles, Los Angeles, CA

A bimorph lithium niobate (LN) transducer has been proposed as a high temperature pressure sensor. Surface electrodes sense the lateral in-plane electric field in thin LN films resulting from out of plane deformation due to pressure. The bimorph is implemented using LN films with opposing polarization, achieved with a wafer bonding approach. We ultimately envision using two thin (~1 μm) LN films on silicon, whereby an approximately 500 μm diameter diaphragm is formed via a backside through wafer etch. This presentation summarizes our preliminary work using thicker LN films (300 μm) and larger diaphragms (6.35 mm diameter). Laser doppler vibrometer (LDV) measurements are performed using piezoelectric excitation of the diaphragm to characterize mode shapes of the diaphragm, and pitch-catch acoustic measurements are performed in air using tone burst waveforms.

LTLT Posters

TA4 – High Performance Digital and Mixed-signal Technologies)

P.35: An 8-Channel On-Chip Multilevel Link with Class-D Analog Buffers Leveraging CDMA/TDMA Multiple Access Schemes

Haris Suhail, Chih-Kong Ken Yang, Sudhakar Pamarti
University of California, Los Angeles, CA

This paper presents a multilevel on-chip link for shared simultaneous communication between multiple nodes through a single metal line. The link utilizes class-D multilevel buffering to buffer the wire and alleviate the length-squared dependence of the wire delay. Two separate links are developed where CDMA and TDMA are employed to enable multiple access. A third link utilizes this technique for on-chip point-to-point communication using PAM8. Fabricated using a 16-nm-class FinFET process, the proposed link is adaptable, allowing data routing to and from various nodes by reconfiguring digital control codes without modifying the analog circuitry. It can also be configured for broadcasting to multiple downstream nodes. The system demonstrates eight independent data channels over a single physical link, achieving high bandwidth efficiency. The design reaches an aggregate data rate of 8 Gb/s with a power efficiency of 150 fJ/bit/mm.

Packaging, Integration, Thermal and Control Technologies Posters

(TA5 – Packaging, Integration, Thermal and Control Technologies)

P.36: How to Minimize Intrinsic Warpage Effects and Conformal Coating Printed Circuit Boards (PCBs) Experiments

ThuHong Tran
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As the scaling technology continues to grow, the smaller components, and thinner multi-layer Printed circuit boards (PCBs) becomes main sources of supplies for portable and wearable products in the electronics industry evolution. The advanced PCBs must shrink the space area and dimension to fit into the advanced stacking assembly process, latent defects and warpage deformation are the most concerns for reliability performance due to the thermal and energy effect through surface mounted components inside PCBs. The DoD relies on commercial-off-the-shelf products, understanding these

reliability concerns of how to minimize the intrinsic warpage is essential to mission readiness. The factors which can reduce the warpage effects, including the coefficient of Thermal Expansion, Glass Temperature, Junction Temperature, and various materials, become important elements for PCBs and IC manufacturers' consideration. The conformal coating PCBs were selected for warpage experiments since they can withstand flexible, durable, UV light absorb and bending in harsh environments

P.37: UCIe Full Signal Integrity Analysis Flow with Compliance Check for Heterogenous Integration

Shawn Mills
Cadence Design Systems, San Jose, CA

Universal Chiplet Interconnect Express (UCIe) standard is important for the future of advanced packaging and semiconductor system design. This paper explores the trends in the industry and Cadence Design Systems complete analysis solutions with UCIe standard compliance checking and verification. This paper details the analysis solution and design architecture with various testcases from Cadence Design Systems and their customers who continually push the industry standards and challenges the existing analysis capabilities currently available.

P.39: Low Pressure HiPIMS+Kick AlN Deposition with Ultra High Growth Rate

Diego A. Contreras Mora, Ping-Che Lee, Aaron McLeod, Andrew Kummel
University of California, San Diego, La Jolla, CA

Mingeun Choi, Satish Kumar
Georgia Tech, Atlanta, GA

P.40: Power and Performance tuning thru the Hedge Technique – Via Intelligent Selection Library Cells for Unique Complex Book

Sebastian Theodore Ventrone, Hayden Clay Cranford
VIEE, Shelburne, VT

This paper presents the VIEE Hedge Technique, an innovative approach for optimizing performance and reducing power consumption in large-scale integrated circuit (LSIC) logic design. By consolidating high-ranking common logic paths into more complex blocks, the VIEE Hedge Technique streamlines circuit design, minimizes redundancy, and maximizes critical path efficiency. The proposed method significantly reduces silicon area and capacitance, leading to lower power consumption, particularly in critical paths. As circuit complexity increases, traditional optimization methods struggle to maintain performance. The VIEE Hedge Technique addresses these challenges by offering a novel approach that overcomes performance limitations while achieving energy efficiency. This paper outlines the development process, expected benefits, and roadmap for implementing the technique across various digital platforms.

P.41: 28 GHz Phased Array Module System-in-Package

Joe Schmelzer
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Matt Bergeron, Myron Cotran, Dat Lam, Rainier Arcena
Integra Technologies, Milpitas, CA

ED2 has designed a 28 GHz Phased Array Module System-in-Package. Integra Technologies worked with ED2 to build the first prototypes of this exciting new product. There were significant learnings along the way by both ED2 and Integra to bring this product to the market.

P.42: Path to an Open Chiplet Ecosystem: A Phased Approach

Salem Abdennadher
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Tao Zhou
Intel, San Diego, CA

Building an open chiplet economy and marketplace, complete with composable and reusable solutions is a multi-year journey with significant technical barriers thanks to divergent standards, lack of compatibility, bottlenecks in testing and validation, plus scalability and futureproofing. An array of technological innovations has paved the way for the emergence of multi-die systems. Building an open chiplet marketplace requires a phased approach, it starts with industry experimentation Phase, followed with customized collaboration phase and ending with chiplets becoming interchangeable phase. This paper will describe the phased approach and present the latest development in standards to enable Open Chiplet economy. We will present different standards initiatives that is helping to enable the final phase of open Chiplet economy: UCIeTM Interop and Compliance, AMBA Chip to Chip (C2C), JPE30 extension and OCP 3DIC Design Kit (3DK) are examples of latest developments enabling the vision of interchangeable chiplets.

P.43: Thermal-Aware Optimization of Distributed Cryogenic Computing Systems

Nurzhan Zhuldassov, Daniel Štefankovič, Eby G. Friedman
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The importance of distributed computing systems has been increasing over the past decade. In a typical data center, 42% of the total power is allocated to thermal management. Increasing the efficiency of the thermal management process can therefore provide significant power savings and lower operational cost. A methodology is proposed to partition a system into groups and select the optimal temperature for each group, enhancing the overall energy efficiency of distributed cryogenic computing systems. The approach proposed here addresses the limitations of previous methods by allowing for a dynamically optimized number of refrigeration stages based on the specific requirements of the system. Units are grouped based on the performance and power profiles, ensuring that each group operates at the most efficient temperature. Both the number of stages and the configuration of the units within those stages are therefore determined based on specific performance constraints, maximizing efficiency while minimizing power consumption.

P.44: Microelectronics and Advanced Packaging Technologies Roadmap

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MAPT REXCOM, Washington DC

Brett Goldsmith
NIWC Pacific, US Navy, San Diego, CA

Informed by SRC’s 2030 Decadal Plan, the MAPT (Microelectronics and Advanced Packaging Technologies) Consortium has developed the MAPT Roadmap, with SRC providing administration, coordination, and expertise. The MAPT Consortium includes 112 organizations with representation from the relevant industry stakeholder across the entire value chain. Participation by academic experts ensures the project is informed by leading-edge science and engineering in key disciplines. There are also government participants from agencies with missions that align with MAPT research and development of advanced manufacturing in ICT. The goal of the MAPT Roadmap is to delineate the technology and performance requirements in microelectronics over the next 15 years, with a special emphasis on packaging and integration.

P.45: Implementation of Field Programmable Gate Arrays (FPGAs) in Extremely Cold Environments for Space and Cryogenic Computing Applications

Christopher Lewis, Drew Sellers, Michael Hamilton
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With the increasing demand for exosphere-bound technologies in communication, large data/AI oriented imaging frameworks, and highly sensitive astronomical space observatories, reliable adaptation of commercial and complex technologies into environments of extreme temperature variations are paramount. In this work, the operation of CMOS Field Programmable Gate Arrays (FPGAs) at extremely cold environments as low as 4 K is demonstrated. Various FPGA and periphery hardware design techniques spanning from HDL design to improvements of peripheral circuitry such as discrete voltage regulators are displayed, and their respective performances are reported. While general operating conditions for voltage regulators are widened, FPGAs see a broader temperature range with improved jitter performance, reduced LUT delays, and enhanced transceiver performance at extremely low temperatures.

P.46: GlobalFoundries and Cadence – Advancing RF/AMS Design for Homogeneous Integration

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Parv Malhotra, Hitesh Marwah
Cadence Design Systems, Noida, India

Mike Lin
Cadence Design Systems, San Jose, CA

Aditya Melinamane Ramesha, Kranti Kumar Tantwai
GlobalFoundries Inc., Bangalore, India

Praveen Pillai
Cadence Design Systems, Austin, TX

Three dimensional systems have moved from publication to productization, but most solutions implemented have been either digital or memory systems. 3D integration will undoubtedly move into the analog mixed signal product domains, but a review of the present EDA and packaging capabilities shows that there are substantial gaps between capabilities to integrate a 3D "digital" solution and what is required to optimize a 3D analog mixed-signal solution. These gaps become particularly apparent for high-frequency and high-performance applications where multiple layers of homogeneous/heterogeneous technologies are required. In this paper we will discuss GlobalFoundries 3D analog Homogeneous/Heterogeneous process "Slate" and RF 3D IC design solution provided by Cadence Virtuoso IC Folding feature and EMX tools.

Photonic Technologies, Components, and Systems Posters

TA6 – Photonic Technologies,Components, and Systems

P.47: Developing Single Short-Pulse RF-Photonic Radar

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This work demonstrated a new RF-Photonic single short pulse Radar concept using an optical fiber recirculation loop based analog correlation method that revolutionizes the signal detection and measurement technique. It provides unprecedented capabilities for the Radar and RF EW systems to operate and detect single short signal pulse to reduce Radar down-time and achieve LPI/LPD.

P.49: High Gain, Energy-Efficient InGaAs/InP Heterojunction Phototransistors

Kehley Coleman, Nathaniel Coirier, Hooman Mohseni
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To address a need for compact, energy-efficient photodetectors which is not met by many currently commercially available technologies such as amplified avalanche photodiodes and PIN detectors, heterojunction phototransistor devices based on electron injection are fabricated from epitaxial III-V semiconductor. These detectors, operating without external amplification at room temperature, exhibit gain of upwards of 300 at low voltage bias of –1.5 Volts and relatively low optical powers (< 30 μW), with very low dark noise close to the fundamental thermal noise limit of $P_{noise} = kT$. Device bandwidths vary from upwards of 20 MHz for large (30 μm) devices to upwards of 200 MHz for the smallest (2 μm). Of particular interest are arrays of parallel 2 um devices forming “multi-injectors” which demonstrate faster device performance compared to single-element devices of similar total active area. Potential applications include systems for high-resolution 3-D imaging and mapping, medical optical imaging, and optical communications.

P.50: A Radiation-Hard Long Range LiDAR SoC for Both Linear and Geiger Mode Avalanche Photodiodes

Megan Manifold, Josh Coffey, Roman Fragasse, Shane Smith, Phillip Barker, Nicholas Wells, Ethan Garrett, Gary Sung, Braden Redick, Grayson Hollaway, Ramy Tantawy
SenseICs Corporation, Columbus, OH

P.51: Edge and Distributed Computing (EDC) Enabled by Co-Packaged Optics (CPO)

Michael T. Hoff, Isaac C. Leffler, Patrick D. Zarnas, Garrett H. Tan, Harsha N. Torke, Rick C. Stevens
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P.52: Co-Packaged Optical Assembly with Detachable Interconnect

Lily Yuan, Fan Fan, Kumar Abhishek Singh, Dekang Chen, Peter A Williams, Darren A Vance, Sunny Situ, Ziyin Lin, Joel Wright, Bilas Chowdhury, Henry Wladkowski, Todd R Coons, Feifei Cheng, Liqiang Cui, Wei Gong, John C Decker, Noe Alarcon, Erasenthiran Poonjolai, John Oh, Saikumar Jayaraman
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On-package optical interconnect is crucial to enable Co-Packaged Optics (CPO) in advanced computing environments where enhanced bandwidth and high performance are essential. The typical approach of “pigtail” fiber array unit (FAU) permanently attached to the photonic IC (PIC) has shown both benefits and limitations. To mitigate the reliability risks inherent to the pigtail FAU and to modularize the package, this study developed a detachable expanded beam connector (EBC) solution on a multi-chip package (MCP) off two tightly spaced PICs. It leverages the proven v-groove fiber attach process and material solution at the die edges and adopts the state-of-the-art EB optical interface on the package edge, making it a viable solution that can transform any existing v-groove based photonic package with pigtail fiber array into one with detachable connector. Furthermore, it is demonstrated that the detachable connector with optimized alignment results in coupling efficiency comparable to directly attached fibers.

P.53: Packaging and Subsystem Integration of a Monolithic Radio Frequency, Photonic, and Digital Integrated Circuit for High-Speed Radio Frequency Processing

Jacob Alward, Christian Bottenfield, John Brooks, Meredith Caveney, Jacob Campbell, Christopher Clark, Christopher Coen, Theodore Franklin, T. Robert Harris, Stephen Hurst, Paul K. Jo, Robert Lingle Jr., Brandon Lovelace, Nelson Lourenco, Peter McMenamin, Robert Moreland, Taylor Peterson, Leif Sandstrom, Billbang Sayasean, Maxwell Tannenbaum, Tucker Turner, J. Glen Vinson, Laura Vinson, Anthony Zenere, Andrew Stark, Benjamin Yang
Georgia Tech Research Institute, Atlanta, GA

Power Electronics and Emerging Power Technologies Posters

TA7 – Power Electronics and Emerging Power Technologies

P.54: High Permeability Ferrite Films on PCBs, Magnetic Substrates, and Related Applications

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Chenyang Zhu, Xin Zhao
Clemson University, Clemson, SC

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Mohan Sanghadasa
US Army DEVCOM Aviation & Missile Center, Redstone Arsenal, AL

The power efficient devices have been proposed for decades. The magnetic PCBs and Si substrates have been widely used in the industries recently, producing smaller sizes, high power efficient, and cost-effective devices. Despite these notable strides, various challenges persist, including large loss tangents, particularly at frequencies exceeding 400–500 MHz, cost intensive manufacturing processes, constrained size and weight parameters, and intricate production procedures. In this work, The spin spray deposition technology is proposed for depositing thick ferrite films onto FR4 PCBs producing high magnetic permeabilities. This technique yields large-size magnetic PCB panels with an enhanced and tunable relative permeability of >100. These new ferrite/PCB laminates exhibit cost-effectiveness, scalability, tunable permeability and permittivity, and better performance metrics. Notably, it also have the potential on the manufacturing high Q, low loss power inductors with high inductance, which has the potential in the application of the high performance computing in the future.

P.55: A Multilevel Drain Supply Modulator Operating from a Single DC Supply

Audrey Cheshire, Paul Flaten, Zoya Popović, Dragan Maksimović
University of Colorado Boulder, Boulder, CO

This paper presents a high-frequency, four-level drain supply modulator (DSM) based on a flying capacitor multilevel (FCML) architecture, designed for envelope tracking in radio-frequency power amplifier applications. Operating from a single dc supply voltage, the proposed FCML-DSM employs a simple state-machine-based active balancing of the flying capacitors and control of the output voltage levels at switching rates up to 25 MHz. A GaN-based hardware prototype of the FCML-DSM is presented with an output voltage range from 0 V to 20 V, discretized into equally spaced levels. It achieves an average efficiency of 95.4% for output powers exceeding 10 W while tracking a 35 MHz 16-QAM signal envelope.

P.56: Radiation Tolerant Silicon Carbide High Voltage Transistors for Switching Power Converters

Akin Akturk, Ethan Mountfort, Mitchell Gross, Bryce Galey, Usama Khalid, Zeynep Dilli
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To achieve massive weight and volume savings in space and high-altitude missions, and to expand the operational range of critical applications, radiation-hardened high voltage and power devices are needed. Therefore, to address the need for radiation-tolerant high voltage power components, we have been developing silicon carbide power MOSFETs that are less susceptible to single event effects, total ionizing dose drift and displacement damage. The single event burnout threshold voltage of these devices has been increased by more than 40% of that of commercial-off-the-shelf components. The total ionizing dose and displacement damage experiments also indicate a conservative radiation tolerance larger than 300 Krad (SiO_2) and 10^{12} p/cm^2, respectively.

P.57: Carrier Lifetime Control Through the Quantum Confined Stark Effect

James Loveless, Vincent Meyers, Luke Yates, Mike Smith, Anthony Rice, Robert Kaplar
Sandia National Laboratories, Albuquerque, NM

This study explores how the quantum confined Stark effect (QCSE) influences minority carrier lifetimes in III-N quantum wells (QWs) by varying the well width. It is found that increasing QW width from zero (bulk material) increases radiative lifetime due to charge separation until charge screening effects reduce and rectify the QCSE for large well widths. Numerical simulation of GaN wells clad with $Al_{0.05}Ga_{0.95}N$ barriers of varying dimension predicts a peak carrier lifetime at a QW width of about 20 nm, with marginal enhancement at widths above 40 nm. Time-resolved photoluminescence (TRPL) measurements on multi QW samples are found to be in reasonable agreement with the numerical findings. Photoluminescence (PL) measurements are also used to observe characteristic red-shifts in the transition energy, which disappear with increased carrier density. The ability to control carrier lifetimes through QW dimensions has significant implications for improving minority carrier GaN and AlGaN devices.

P.58: Towards Improved Ohmic Contacts to P-type Nanocrystalline Diamond Films

Audrey Rose Gutierrez
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Tatyana I. Feygelson, Bradford B. Pate, Alan G. Jacobs, Marko J. Tadjer, Karl D. Hobart
U.S. Naval Research Laboratory, Washington, DC

Nanocrystalline diamond (NCD) is a promising thin film semiconductor that is possible to dope highly p-type with Boron while retaining its high thermal conductivity when grown sufficiently thick. In this work, Al was investigated as an Ohmic contact metal to NCD with Ti and 1–2 nm thick B_4C contact layers. For a 4 sccm B_2H_6 doped NCD layer, the specific contact resistivity of simple Al and all bilayer contacts were of order 10^{-2} Ω-cm^2, contacts with a B_4C interlayer exhibiting the lowest contact resistance. After annealing at 600 °C for 1 minute in N_2 however, the Ti/Al metal stack improved ~2.5 orders of magnitude compared to ~1 order of magnitude for other film stacks.

P.59: Tactical Grid Enhancement: Advancements in Power Electronics and Low Earth Orbit Satellites Enable System-of-Systems Near-Real-Time Control

Nicholas B. Leak, Fang Luo
Stony Brook University, Stony Brook, NY

This research addresses the modernization of military defense through a Fleet Tactical Grid System-of-Systems (SoS) approach, focusing on managing power margin to accommodate the integration of advanced Directed Energy (DE) systems in power-constrained mobile platforms such as ships and aircraft. The proposed SoS employs three communication and control strategy levels, Primary, Secondary, and Tertiary, to near-real-time control through coordination and synchronization with dedicated GPS time servers. This framework extends mobile unit electrification beyond previously explored system-level control. It aims to overcome the limitations of current individual systems in handling multiple threats simultaneously by enhancing inter-vessel coordination of DE power distribution. An industrial communication protocol facilitates precise synchronization, allowing for power margin gains when needed during defense engagements and allocates assignment of threat mitigation accordingly.

Radiation Hardened Technologies, Designs, and Systems Posters

(TA8 – Radiation Hardened Technologies, Designs, and Systems)

P.60: System-Level Fault Injection on Heterogeneous System-on-Chips

Edward Carlisle IV, James Koiner, Evan Ezell, Scott Harper
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This paper presents a system-level approach to fault injection on heterogeneous System-on-Chip devices. Our approach simultaneously targets multiple resource types while taking care to maintain transparency of the fault injector and minimizing constraints on the end user design. Our approach integrates with the Benches' platform to enable fully automated operation and provide campaign analysis features. The platform can also be leveraged to automate radiation testing.

P.61: Single Event Effects Characterization of PWM and ADC Modules of TI TMS320F28377D Microcontroller

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University of Texas at Dallas, Richardson, TX

Matthew Pate
Texas Instruments Incorporated, Sugar Land, TX

There is an increasing demand to use commercial-off-the-shelf (COTS) microcontrollers for space applications. These hardware, in the presence of radiation, are vulnerable to single event effects (SEEs). We report on the SEEs and reliability of a Texas Instruments TMS320F28377D microcontroller. Our goal is to develop robust test methodologies for characterizing the space radiation vulnerabilities of mission-critical MCU peripherals. Using a unique strategy developed for each peripheral, we analyze reliability using the captured SEE data. Test isolation of individual on-chip components is achieved using physical masks that expose only the module under test to ionizing radiation. The proposed system health tracking mechanism (respective to each module under test) leverages the microcontroller architecture (reading control registers) to monitor the system's state. The results of this experiment allow us to observe the SEEs and perform reliability analysis of on-chip modules — ADC and ePWM of the TMS320F28377D MCU.

P.62: Neutron Radiation In-Situ Failure-in-time Characterization of 1200 V–1700 V SiC Power Transistors

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Stephen Arthur Wender, Kranti Gunthoti
Los Alamos National Laboratory, Los Alamos, NM

This work is focused on the reliability testing of wideband gap (WBG) SiC power transistors due to terrestrial neutron radiation. Wide bandgap SiC power transistors are attractive candidate for aerospace and satellite communication which offer smaller footprint, lower weight, higher-temperature operation, lower power losses, and higher operating frequency. We have tested 1200 V–1700 V power transistors with/ without high temperature, and with/without angular placement in this work. The devices were in-situ tested for failure-in-time (FIT) analysis method at Los Alamos Neutron Science Center (LANSCE) in ICE House-1 facility at a flux of 10^6 n/cm^2-s above 1.5 MeV energy. The FIT values in room temperature showed higher numbers than the 150 C and 100 C values. The FIT values at different angular placements (30, 45, 90) showed exhibit greater variance at non-zero angle, and a slight decrease as the incidence angle approaches 90.

P.63: Magnetoresistive Random Access Memory (MRAM) for Radiation Hardened Applications

Romney R. Katti
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Magneto-resistive Random Access Memories (MRAMs) are of key interest to government microcircuit applications. MRAMs apply critical technologies to provide radiation hardened non-volatile memories (NVMs) with high to unlimited write and read cycling and long to unlimited data retention times over long specified lifetimes typically exceeding fifteen years with broad temperature ranges, low error rates, and latch up and single-event fault interrupt (SEFI) immunity. Radiation hardened toggle-bit MRAM operating principles, technology, products, test results, and developmental MRAMs at the 150 nm node will be discussed, along with radiation hardened Spin Transfer Torque (STT) MRAM devices, technology, and operating principles being developed at the 90 nm node to develop a 64 Mb STT-MRAM in a single-chip package (SCP) and 256 Mb and 512 Mb STT-MRAM Multi-Chip Modules (MCMs) using radiation hardened 64 Mb STT-MRAM die.

P.64: A Radiation Hard Reconfigurable Analog Front-End Array Optimized for High-Speed Performance and Detector Capacitance

Nicholas Wells, Roman Fragasse, Phillip Barker, Megan Manifold, Ethan Garrett, Gary Sung, Ramy Tantawy, Shane Smith
SenseICs Corporation, Columbus, OH

Waleed Khalil
The Ohio State University, Columbus, OH

RF Technologies, Components, and Systems Posters: Advanced RF Components & Devices
(TA9 – RF Technologies, Components, and Systems)

P.65: Integrated Magnetoacoustic Isolators with Giant Non-Reciprocity

Bin Luo, Yisi Liu, Ben Davaji, Nian-Xiang Sun
Electrical and Computer Engineering Department, Northeastern University, Boston, MA

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Integrated nonreciprocal isolators and circulators have revolutionized wireless communication and sensing. Recently, integrated magnetoacoustic non-reciprocal RF devices are emerging as a transformative solution for low-power, wideband full-duplex wireless communication systems, addressing the limitations of conventional nonreciprocal isolators and circulators that demand high power consumption. Despite notable advancements, high insertion losses, particularly at GHz frequencies, have remained a critical challenge. In this study, we present a magnetoacoustic non-reciprocal RF device operating at 2.87 GHz in the fundamental SAW mode, achieving a significant reduction in insertion loss to 10 dB at 2.87 GHz and demonstrating an exceptional non-reciprocity of 200 dB/mm at multiple acoustic resonance peaks near 2.95 GHz. These results underscore the device's potential as a compact, power-efficient solution for next-generation RF isolators and circulators, with broad implications for advanced wireless technologies.

P.66: PCB-embedded Circulators for Modern RF Frontend Applications

Thomas Lingel, Matthew Edlich, Tyler McGrath
TTM Technologies, East Syracuse, NY

Frontend designs that are used, for example, in active electronically scanned arrays (AESA), need to meet demanding requirements such as low insertion loss, adequate power handling capabilities, and linearity. In some cases, full duplexing functionality is required. Typically, switches are employed due to size constraints that lead to performance drawbacks and prevent full duplex operation. Passive circulator devices based on nonreciprocal properties established by microwave ferrites offer desired capabilities but are more expensive and require more real estate. An integrated printed circuit board (PCB) packaging concept for ferrite circulators is introduced, offering significant performance advantages at a reasonable size and cost. The concept is further expanded to integrate a stacked double junction circulator.

P.67: Performance of Off-the-Shelf Diodes Used as Sharpeners in Picosecond Pulse Generators

Alex Usenko
University of Missouri Kansas City, Kansas City, MO

RF Technologies, Components, and Systems Posters: Algorithms, EDA Tools for Modeling, Analysisx & Fabrication
(TA9 – RF Technologies, Components, and Systems)

P.71: An Integrated Design Flow to Simplify 3DHI RF/ Microwave Cross-Fabric Analysis

Daniel Schlieter, Jason Kehl, Ted Hoffman
Raytheon, An RTX Business, McKinney, TX, El Segundo, CA, Hannover, MD

Harsha Hakkal, Kerry Judd, Jim Donley, Brian Hirasuna
Cadence Design Systems, Inc., San Jose, CA

As 3-D heterogenous integration (3DHI) becomes state-of-practice, designers must consider the RF/microwave performance through the cross-fabric of the integrated circuit (IC), package, and board. Existing 3DHI design and analysis flows utilize inefficient, costly, and error prone methods such as chopping-up designs to reduce complexity, maintaining multiple design databases across tools, and assigning common reference planes to design through technologies. These methods sometimes result in duplicated work, confusion over design analyzed or fabricated, increased area required, and reduced performance. This paper presents a new methodology, the Virtuoso RF Solution (VRF), to simplify 3DHI RF/microwave cross-fabric design and analysis. VRF reduces complexity by using a single cockpit to manage designs across databases, tools, and technologies. The VRF cockpit assists the designer to speed up and simply analysis with net selection, port generation, and layout shape preprocessing. The VRF cockpit also enable cross-fabric co-design with automated model generation and round-trip data exchange.

RF Technologies, Components, and Systems Posters: Power Amplifiers
(TA9 – RF Technologies, Components, and Systems)

P.72: High Performance Dual-Band Concurrent GaN Power Amplifier for 28 GHz/39 GHz Radar and 5G Applications

Swarup Chakraborty, Tian Xia
University of Vermont, Burlington, VT

In this paper, a 28 GHz/39 GHz dual-band monolithic microwave integrated circuit (MMIC) GaN power amplifier has been proposed for the long-range millimeter-wave radar and 5G communication applications. The amplifier integrates a driver and a power circuit, utilizing a commercial 40 nm GaN technology. Unique low-loss dual frequency matching circuits are employed to ensure high efficiency at the desired output power. The similation results show that the power amplifier achieves a saturated output power of 30 dBm at both frequencies, with a power-added efficiency (PAE) exceeding 39%.

P.73: A 3–4 GHz Digitally Reconfigurable Outphasing Transmitter

Josh Coffey, Ramy Tantawy, Megan Manifold, Gary Sung, Grayson Hollaway, Nicholas Wells, Dale Shane Smith
SenseICs Corporation, Columbus, OH

Dominic Mikrut, Patrick Roblin, Waleed Khalil
The Ohio State University, Columbus, OH

Jonathan Ashdown
USAF AFMC AFRL/RITGB, Rome, NY

Poster Session
(TA9 – RF Technologies, Components, and Systems)

RF Technologies, Components, and Systems Posters: RF Subsystems

P.74: A Decade Bandwidth, Dual-Polarized, Steerable Array System Solution with Time Delay Beamsteering

Pedro Rodriguez-Garcia, Jeff Murphy, Colin Dallas
L3Harris Technologies, Rockwall, TX

The Advanced Aperture Solutions (AAS) team at L3Harris Technologies presents a decade bandwidth, multi-mission, steerable array system which operates over the UHF-C frequency bands. This multi-octave system is composed of a scalable 256-element dual-polarized Antipodal Vivaldi Antenna Array (AVAA), and a small form factor true time delay (TTD) beamformer. The pairing of the AVAA with TTD beamformers provides a radio agnostic front end with beam scanning capability that can support a range of applications such as synthetic aperture radar (SAR), signals intelligence (SIGINT), measurement and signature intelligence (MASINT), and telemetry (TM) applications. This capability reduces platform modification cost through sensor reuse and allows a one-time installation to augment roll-on/roll-off transceivers as mission requirements change.

P.75: System Budgeting to System Realization – A 14 nm FinFET 48 GHz FEM for Next Generation 5G/6G Applications

Ritabrata Bhattacharya
Cadence Design Systems, Noida, India

Gent Paparisto
Cadence Design Systems, San Diego, CA

David Vye
Cadence Design Systems, Newburyport, MA

A comprehensive top-down system design methodology is presented and demonstrated with a Front-End Module (FEM)/Antenna-in-Package (AiP) co-design for next generation 5G mobile applications targeting 47 GHz–48 GHz, the n262 band. A link budget analysis of the FEM in a system simulator is carried out to determine block level specifications while adopting package and PCB floor-planning and thermal challenges early in the design. The co-design of the FEM with the packaged antenna is further implemented on a Samsung's 14 nm FinFeT process, with a focus on very low power, low noise amplifiers and p-FinFET based architectures as an alternate to the n-FinFeT architecture for reliable power amplification at mmWave. The integrated chip/package system verification leads to improved correlation between simulation and measurements of the FEM. A unified chip, package and PCB co-design methodology is also presented to highlight the importance of heterogeneously integrated analysis and workflows to enable first pass silicon success for advanced mmWave applications.

P.76: An Overview of Recent Flat-Panel Active Electronically Scanned Phased Array Research at the San Diego State University

Satish K. Sharma, Sanghamitro Das
San Diego State University, San Diego, CA

Jia-Chi S. Chieh
Naval Information Warfare Center Pacific, San Diego, CA

This article presents the details of some of the latest flat-panel active electronically scanned phased arrays (AESA) that were designed and developed at the Antenna and Microwave Laboratory (AML), San Diego State University. The described research works were conducted in collaboration with Naval Information Warfare Center Pacific (NIWC-PAC); United States Army Command, Control, Communication, Computers, Cyber, Intelligence, Surveillance and Reconnaissance (C5ISR) Center; and National Aeronautics and Space Administration Glenn Research Center (NASA-GRC).

P.112: Flight Test Results for Quadcopter UAS Sensor Payload

Nathan Blood
ARA, North Billerica, MA

SPCE Posters

(TA7 – Power Electronics and Emerging Power Technologies)

P.77: In-Circuit Evaluation of High-Performance E-Mode GaN FETs for use in Multistage Point-of-Load Power Converters

Aarranon Bharathan, Dragan Maksimović
University of Colorado – Boulder, Boulder, CO

Antuwon H. Butler, Michael Podel
Lockheed Martin, Grand Prairie, TX

Robert Strittmatter, Sean Morrison
EPC Space, Andover, MA

P.78: Scaling Lateral Superjunction HEMTs and Their Radiation Response

Wiley Yu, Jeongkyu Kim, Thomas Rodriguez, Rohith Soman, Srabanti Chowdhury
Stanford University, Stanford, CA

P.79: High-Density Radiation-Hardened Point-of-Load (PoL) Power Conversion Using Hybrid-Switched-Capacitor Circuit Topologies

Nathan Ellis
University of California, Santa Cruz, Santa Cruz, CA

Eric Faraci
IR HiRel, an Infineon Technologies Company, Andover, MA

Leora Peltz
The Boeing Company, Huntington Beach, CA

Robert Pilawa-Podgurski
University of California, Berkeley, Berkeley, CA

This poster will present recent innovations in power converter circuit topology; namely that of high-performance hybrid-switched-capacitor (HSC) ladder-type structures. Due to both their best-in-class (minimized) switch stress, and recent advancements in structural design, this power conversion technology is on track to become highly competitive for use in radiation-hardened point-of-load (PoL) converters, including direct 48 V-to-1 V conversion. This work will offer brief analytical justification, followed by discussion of current state-of-the-art HSC designs, their conceptual evolution, and roadmap towards industrial adoption in aerospace applications. As part of ongoing development, one promising converter topology will be showcased as a discrete hardware prototype, with measured results demonstrating interleaved pulse-width-modulated (PWM) voltage regulation and both excellent power density and efficiency at a 50 W power level.

THREADS Posters

(TA2 – Emerging Technologies)

P.80: DARPA THREADS Dual Diamond Ultra-Power HEMT Devices

Vincent Gambin, Carolina Adamo, Russell Rioux, Ioulia Smorchkova, Robert Coffie, Nicholas Tanen, Thomas R. Young, Connor Bailey, Andrew Carter, Floyd Oshita
Northrop Grumman, Redondo Beach, CA

Kyeongjae Cho
University of Texas at Dallas, Richardson, TX

Srabanti Chowdhury
Stanford University, Stanford, CA

Trusted, Assured and Cyber-secure Microelectronics Posters

(TA10 – Trusted, Assured and Cyber-secure Microelectronics)

P.81: Verification and Localization of Asynchronous Reset-based Security Vulnerabilities in SoCs

Samit Miftah, Kanad Basu
University of Texas at Dallas, Richardson, TX

P.82: How Lightweight is ASCON Compared to AES? A Detailed Analysis

Eslam Tawfik, Islam Elsadek, Sayed Elgendy, Sherif Abouzeid, Ahmed Ghonem
The Ohio State University, Columbus, OH

John Ross Wallrabenstein, Erik MacLean, Doug Gardner
Analog Devices, Indiana, IN

Sohrab Aftabjahani, Rosario Cammarota
Intel Corperation, Oregon, OR

NIST selected ASCON as the standard Lightweight Cryptography (LWC) algorithm in 2023. ASCON's implementations promise bringing lightweight Authenticated Encryption (AEAD) to resource-constrained devices surpassing Advanced Encryption Standard (AES) implementations. In this work, a standard compliant ASCON Application Specific Integrated Circuit (ASIC) hardware (HW) is designed and fabricated using CMOS GF22FDx technology. ASCON ASIC HW is compared with a standard HW implementation of the AES fabricated over the same chip. ASCON uses only 39% of AES's area and boosts energy efficiency by up to 25 times. To the best of our knowledge, this work is the first work providing a silicon-based analysis for ASCON ASIC implementation reaching a throughput of 4.3 Gbps @ 0.8 V and 2 Gbps @ 0.6 V, and energy efficiency of 1.9 Tb/J @ 0.8 V and 3.5 Tb/J @ 0.6 V in 2505 μm^2 on GF22FDx at 620MHz @ 0.8 V.

P.83: Programmable and Compact Hardware Design for ASCON AEAD and Hash Functions

Eslam Tawfik, Islam Elsadek
The Ohio State University, Columbus, OH

NIST finalized the LWC standardization process, which was initiated in 2018, by selecting ASCON as the new standard. ASCON is a lightweight cryptography algorithm supporting two main functions – AEAD and HASH. ASCON features three AEAD variants – ASCON-128, ASCON-128a, ASCON-80pq – and two HASH variants – HASH, HASHa. In this work an efficient programable hardware design that supports all the three AEAD and two HASH variants is proposed and implemented over GF12nm ASIC technology and Spartan-7 FPGA. The programable design is compared to the HW of each individual variant showing the savings in utilizing the programable design which

eliminates the need for five separate standalone designs. Metrics compared are area, throughput and energy consumption. Results show that the programable ASCON saves 61% of total silicon area. The programable HW has an average energy consumption overhead of 4% compared to dedicated HW design for each variant.

P.84: System in Package and System on Chip Methodologies of Packaging to Address Integration and Security Objectives

Mark Santoro, Krishna Shivaram
Raytheon Technologies, El Segundo, California, CA

P.85: Enhancing Malware Detection with Advanced Machine Learning Techniques and Hardware Performance Counters: A Scalable, Low-Overhead Approach

Xiangrong Zhou, Leonid Meyerovich
Trusted Science and Technology Inc., Rockville, MD

Houman Homayoun
University of California, Davis, Davis, CA

The growing sophistication of malware presents significant challenges to existing detection methods. A more efficient, accurate, and cost-effective approach is needed for next-generation protection. Hardware Performance Counters (HPCs), which access low-level hardware data, have emerged as valuable tools for monitoring software behavior. This paper integrates advanced machine learning techniques into hardware-assisted malware detection, leveraging HPCs to reduce detection latency, minimize overhead, enhance accuracy, and lower false positive rates. Our approach employs deep learning and ensemble models to detect subtle patterns in hardware data. To simulate real-world scenarios, we implement an automated test bench for data collection and malicious series generation, enabling realistic and secure malware detection evaluation.

P.86: Transition of DSSoC-EPOCHS Methodology

Pradip Bose, Augusto Vega
IBM T.J. Watson Research Center, Yorktown Heights, NY

Luca Carloni, Ken Shepard
Columbia University, New York, NY

Sarita Adve, Vikram Adve, Sasa Misailovic
University of Illinois at Urbana-Champaign (UIUC), Siebel Center for Computer Science, Urbana, IL

David Brooks, Gu-Yeon Wei, Vijay Janapa Reddi
Harvard University, Allston, MA

P.87: What to Redact? Guidelines for Cost-Effective Hardware Intellectual Property Protection

C. Sathe, A. Fowler, C. Sechen, B. Carrion Schaefer, Y. Makris
University of Texas at Dallas, Richardson, TX

M. Zaman, R. Narumi
Raytheon, An RTX Business, McKinney, TX

With most Integrated Circuit (IC) design companies now being fabless, methods to protect their hardware Intellectual Property (IP) from unauthorized use or copying have become imperative. In response, the hardware security community has been investigating the concept of hardware redaction, wherein sensitive portions of a design are mapped to an embedded programmable fabric, while the rest of the design remains in ASIC implementation. The bitstream of the programmable fabric, which is not visible to the untrusted foundry, serves as the key for instating circuit functionality. Given the regular structure and universal nature of such fabrics, hardware redaction is impervious to known attacks. The obvious drawback of hardware redaction, however, is the non-negligible area, power and performance overhead

associated with embedded programmable fabrics. In this work, we discuss a set of general guidelines to assist designers in deciding what to redact in order to achieve sufficient protection while ameliorating overhead.

P.88: Large-Area Nondestructive Integrated Circuit Imaging using X-Ray Laminography

Nina Weisse-Bernstein, Yancey Sechrest, Adra Carr, Kevin Mertes, Christine Sweeney, Brendt Wohlberg, John Barber, Michael McCann, Robert Rhodehouse, William Ward, James Hunter, Steven Honig
Los Alamos National Laboratory, Los Alamos, NM

Jeffrey Klug, Yi Jiang, Hanna Ruth, Ashish Tripathi Steven Henke, Michael Roberts, Stefan Vogt
Argonne National Laboratory, Argonne, IL

Richard Sandberg
Brigham Young University, Provo, UT

P.89: Bump-on-Wire: Dual-Use Secure Communications Across Untrusted Networks

Matthew Areno
Intel Corporation, Austin, TX

Joshua Fryman
Intel Federal, Hillsboro, OR

Communications between any two devices not on the same network are likely to cross one, or more, untrusted networks. Existing industry protocols provide attestation of devices and encryption of data but do so at the risk of subjecting the devices containing the associated cryptographic key to attacks by nefarious actors. Additionally, the attestation provided does not prove the actual identify or physical security of the devices. Any device with the cryptographic key(s) can be used in the communications, including one that extracted such keys via unauthorized means. The Bump-on-Wire (BOW) solution is designed to significantly address these concerns by utilizing hardware-unique key derivation, physically partitioning access to cryptographic material, and ensuring an industry-leading security posture. In this presentation, we will provide detailed information on the system security, cryptographic protections, and physical design that are used to ensure post-quantum secure communications between any two devices across any communications fabric.

P.90: ML-PREMISE: A Machine Learning-Driven Pre-Silicon Electromagnetic Fault Injection Security Evaluation for Robust IC Design

Pantha Protim Sarker, Rakibul Hassan, Farimah Farahmandi, Mark Tehranipoor
University of Florida, Gainesville, FL

Tianze Kan, Jingchen Liang, Ozgur Tuncer, Bo He, Lang Lin, Norman Chang
Ansys, San Jose, CA

Electromagnetic fault injection (EMFI) poses a significant threat to the security and reliability of integrated circuits (ICs), potentially leading to data corruption, system failures, or sensitive information leakage. This work proposes a novel machine learning-driven framework for efficient EMFI analysis in pre-silicon IC design. This approach accurately predicts induced currents and their impact on the IC's performance. A key advancement of this work is using machine learning to identify "cutout" regions, which greatly reduces simulation runtime without compromising accuracy. The framework trains a metamodel using a comprehensive dataset of various metal layer configurations and coil distances. By applying and analyzing dynamic current distribution across metal layers, the method evaluates the robustness of the design against EMFI-induced timing violations and faults, offering a practical and efficient solution to enhance the security and reliability of IC designs in the pre-silicon phase.

P.92: Gray-box SoC Hardware Penetration Testing Using Reinforcement Learning and PSO

Hasan Al Shaikh, Shuvagata Saha, Sujan Kumar Saha, Farimah Farahmandi, Mark Tehranipoor, Fahim Rahman
University of Florida, Gainesville, FL

Kimia Zamiri Azar
University of Central Florida, Orlando, FL

System-on-Chip (SoC) hardware verification is inherently challenging due to the ever increasing design complexity, an expanding threat surface, and the presence of third-party IP cores (3PIP) for which full knowledge of the internal structure and functionality (i.e., white-box knowledge) may not be available. However, majority of hardware verification methods popular in industry and academia presuppose white-box knowledge and therefore, do not properly address verification needs in today's SoC development landscape. Hardware penetration testing (pentest) is an emerging hardware verification method inspired by software security practices, but state-of-the-art techniques suffer from suboptimal vulnerability detection speed. This paper addresses this issue by combining the artificial intelligence of reinforcement learning agents and Binary Particle Swarm Optimization (BPSO) in a novel pentest framework. Proposed framework is capable of generating smarter test patterns that target security-critical areas of a design, achieving up to 3× faster detection speed and greater consistency compared to state-of-the-art pentest techniques.

P.93: X-DFS: An Explainable Artificial Intelligence Guided Framework for Design-for-Security

Tanzim Mahfuz, Prabuddha Chakraborty
University of Maine, Orono, ME

Swarup Bhunia
University of Florida, Gainesville, FL

Modern semiconductor supply chain has been designed to boost production efficiency but is filled with major security concerns such as malicious modifications (hardware Trojans), reverse engineering (RE), and cloning. Digital systems are also subject to threats such as side channel attacks. Many Design-for-security (DFS) solutions have been proposed to deal with these vulnerabilities and such solutions (DFS) relays on strategic modifications of the digital designs. However, most of these DFS strategies lacks robust formalism, are often not human-understandable, and require extensive amount of human effort. We propose X-DFS, an explainable Artificial intelligence (AI) guided DFS solution-space exploration approach that can dramatically cut down mitigation strategy development/use time while enriching our understand of the vulnerability by providing human-understandable decision rationale. We implement X-DFS and evaluate it for reverse engineering threats (SAIL, SWEEP, OMLA) and formalize a generalized mechanism for applying X-DFS against other threats.

P.95: SSLF: Automated Static Security Linting Framework for SoC Verification

Rasheed Kibria, Jeremy Lee
Caspia Technologies, Gainesville, FL

Modern system-on-chips (SoCs) are increasingly vulnerable to security threats due to their complexity. To address this, security verification must start early in the design phase. The control path, typically implemented with finite state machines (FSMs), and the datapath may be prone to fault injection, denial-of-service (DoS) attacks, or information leakage. Bad design practices at the RTL stage can lead to these vulnerabilities. This paper introduces SSLF, a static analysis-based security linting framework that checks for violations of security guidelines. Experiments on an open-source SoC design demonstrate SSLF's effectiveness in identifying potential security issues.

P.96: Voltage-Independent Crosstalk Metrics using a Ring Oscillator Locking Phenomenon in FPGAs

Austin Davis, Casey Fendley, David Fatheree, Joel Bjornstad, and Seth Cohen
Kratos SRE, Inc., Birmingham, AL

P.97: Advancing Microelectronics Assurance while Preserving Confidentiality: Copia

Nikhil S. Shenoy, Kelly E. Glebus
Colvin Run Networks, Inc., Tysons, VA

Nicholas Pattengale
Sandia National Laboratories, Albuquerque, NM

Nathan J. Edwards
Rapid Innovation & Security Experts, Inc., Colorado Springs, CO

Cameron Patterson
Consultant, Bemidji, MN

Evan M. Lally, Tyler E. Olson
Dogwood Logic, Inc., Blacksburg, VA

We sketch two contrasting schemes whereby a party wishing to verify a purchased microelectronic, can compare their independent measurements with measurements made by the manufacturer during fabrication, without requiring the manufacturer to divulge proprietary information. This paper also discusses the trade-offs and pathway toward technology adoption.

P.98: Leveraging Commercial EDA Technology to Perform Independent Verification or Certification of FPGAs Used in Critical DoD Systems

Jonathan Frey
Booz Allen Hamilton, McLean, VA

James McKay
Booz Allen Hamilton, Rome, NY

Mark Labatto
Booz Allen Hamilton, Beavercreek, OH

Adam Sherer
Cadence Design Systems, San Jose, CA

Matthew D. Sale, Kevin J. McCamey
Air Force Research Laboratory, Wright-Patterson AFB, OH

P.99: SCA-Protected HW/SW Co-Design of Post-Quantum Stateful Hash-Based Signatures

Abubakr Abdulgadir, Reza Azarderakhsh, Luke Beckwith, Rami Elkhatib, Duc Tri Nguyen
PQSecure Technologies, LLC, Boca Raton, FL

As quantum computing grows, current cryptographic algorithms become vulnerable, making post-quantum cryptography (PQC) essential. Hash-based signature schemes are promising for their quantum resistance, but purely software (SW) or hardware (HW) implementations face challenges. SW-only offers flexibility but lacks performance, while HW-only provides speed up and efficiency demanding adaptive designs for different parameters. SW/HW co-design balances these trade-offs, combining software's adaptability with hardware's speed. Our side-channel attack protected SW/HW co-design achieves an eight to ten time speed improvements over software-only implementations without side-channel protections. This approach simplifies state management, algorithm updates, and optimal security design, making it ideal for quantum-resistant code signing, software updates, and root-of-trust.

P.100: Security-Aware Reconfigurable Interposer (SARI): Building Secure Systems out of Untrusted Chiplets

Michel A. Kinsy, Eric J. Jahns
Secure, Trusted, and Assured Microelectronics (STAM) Center, Arizona State University, Tempe, AZ

Heather R. Kinsy
Secure Micro Technologies, LLC, Phoenix, AZ

P.101: GenP: Harnessing Generative Properties for Hardware Security Verification

Avinash Ayalasomayajula, Md Rafid Muttaki, Jeremy Lee
Caspia Technologies, Gainesville, FL

As system-on-chip (SoC) complexity grows, ensuring security becomes increasingly challenging. Formal verification helps model and check security properties, but generating these properties manually is labor-intensive. This paper presents GENP, an AI-powered framework that automates the generation of security properties from Register Transfer Level (RTL) designs. By leveraging large language models (LLMs), GENP extracts key features and security assets from RTL and specifications, generating tailored security properties. These properties are output in both natural language and SystemVerilog assertions (SVAs) for formal verification and stored in a security property database, enhancing future verification efforts efficiently.

P.102: Assessing Physically Unclonable Functions for Anti-Tamper Applications

Nick Egbert
Mercury Systems, West Lafayette, IN

Jon Mellott
Mercury Systems, Gainesville, FL

Dan Toohey
Mercury Systems, Andover, MA

Despite the growing research in the space of physically unclonable functions (PUFs), the defense industry lacks guidance on how to evaluate PUFs for anti-tamper applications. In this paper we explore the various qualities a tamper-resistant PUF should ideally possess and how some of these qualities may be metricized.

P.104: A Case Study on Low-cost Pre-Silicon Side-Channel Analysis of CRYSTALS-Dilithium

Jasper van Woudenberg, Cees-Bart Breunesse
Riscure Security Solutions, Keysight, Santa Rosa, CA

This case study presents a methodology for performing pre-silicon side-channel analysis (SCA) on large cryptographic algorithms like Dilithium, a post-quantum cryptography (PQC) scheme. Traditional tools struggle with such algorithms due to their large gate counts and high clock cycle demands. By integrating Gate-Level Information Flow Tracking (GLIFT) and leveraging cloud-scaling techniques, we demonstrate a reduction in the computational overhead and cost required for analysis. Our approach reduces the number of signals to 5.6% and compresses time intervals to 30.8% of the original, achieving analysis runtimes of under 24 hours for under USD800. The scalability and speed of this method make it a viable solution for practical use.

P.105: Accelerating Microelectronics Digital Design for Digital Engineering

Ryan Walker, Kyle Ahearn, Cronus Dillard, Mark Vlassakis, Mark Labbato
Booz Allen Hamilton, Beavercreek, OH

Jamin J. McCue, Vipul Patel, Kevin J. McCamey, Matthew D. Sale
Air Force Research Laboratory, WPAFB, Ohio

P.106: Design Recovery Workflow for Legacy Integrated Circuits Via Optical Image Feature Extraction

Timothy McDonley, Jon Scholl, Noah Padro, Yash Patel, John Kelley, Adam Waite, Noah Taylor, Nicholas Harner, Preston Pozderac, Emily Haines, Adam Kimura
Battelle Memorial Institute, Columbus, OH

Tamara Juntiff, Christian Eakins
Air Force Research Laboratory, Dayton, OH

P.107: Library-Attack: Reverse Engineering Approach for Evaluating Hardware IP Protection

Aritra Dasgupta, Sudipta Paria, Swarup Bhunia
University of Florida, Gainesville, FL

Christopher Sozio, Andrew Lukefahr
Indiana University, Bloomington, IN

Existing countermeasures for hardware IP protection, such as obfuscation, camouflaging, and redaction, aim to defend against confidentiality and integrity attacks. However, under the current threat model, these techniques overlook the possibility of an adversary with highly specialized expertise and authorized access to the supply chain who can leverage privileged information about the protected designs and the countermeasures used to recover the original design from a library of unprotected designs with similar functionality. To address this scenario, we introduce Library Attack, a novel methodology for reverse engineering hardware IP leveraging a library of unprotected designs along with prior knowledge of the employed security countermeasures. The designs from the library are transformed, and their structural properties are compared using commercial EDA tools. We demonstrate how Library Attack can be used to compromise existing hardware IP countermeasures using ISCAS89 benchmarks.

P.108: A Novel Electronic Design Automation (EDA) Tool for the Design of Cyber-Secure Microelectronics

Joseph Lenhart, Christopher S. Diltz, Vasker Bhatacherjee, Andrew Szabo
Edaptive Computing Inc., Dayton, OH

Paul Wong
Defense Microelectronics Agency, McClellan Park, CA

Over the last 30 years, there has been a rapid change for both design and verification across the microelectronics landscape. With design complexities has come a need to perform robust design verification and assurance across different levels of design abstraction, including Register Transfer Level (RTL), synthesized netlists and post silicon manufacturing. Assertion-Based Verification (ABV) is a commercial best practice which imbeds non-synthesizable checkers into the Register Transfer Language (RTL) to verify internal functionality of Application Specific Integrated Circuits (ASIC's) and Field Programmable Gate Arrays (FPGA's). This paper describes the concept of synthesizable assertions imbedded in RTL code to be used for assurance and cyber-security of ASIC and FPGA hardware to detect unintended or malicious functionality. The resulting solution will augment the DoD's existing verification methodologies with automated, sustainable workflows, enabling reduction in manual error, and ensuring digital designs meet functional, safety and security requirements on ASIC and FPGA platforms.

P.110: Towards Synthetic Data Generation for Characterization of FPGAs

Whitney Batchelor, Cody Crofford, Margaret Winslow, Mia Taylor, Kevin Paar, James Koiner, Scott Harper
Graf Research Corporation, Blacksburg, VA

Both the increasing use of machine learning to reason over features relevant to microelectronics and the ongoing threats to the microelectronics supply chain necessitate the need to explore novel methods for characterizing and identifying known good microelectronic devices. Synthetic data generation for use in machine learning training is growing in popularity but comes with its own set of challenges. We present a method for synthetically generating field programmable gate array data that can not only be used to train models for our FPGA counterfeit device detection solution, but generally used as characterization data for known good FPGAs.

P.111: An Efficient Number Theoretic Transform Implementation for CRYSTALS-Kyber on FPGA

Eslam Tawfik, Sherif Elewa
The Ohio State University, Columbus, OH

The Number Theoretic Transform (NTT) is widely adopted in modern Post-Quantum Cryptography (PQC) systems due to its ability to perform polynomial multiplication efficiently. Among these systems is the CRYSTAL-Kyber as a Module-Lattice-based Key Encapsulation Mechanism (ML-KEM). It involves various complex operations including polynomial modular multiplication with modulo $q = 3329$. In this work, an efficient conflict-free addressing NTT architecture with a modified Barrett-based modular reduction for CRYSTAL-KYBER is introduced to significantly reduce the hardware area, while maintaining high performance. The proposed NTT design is implemented on Xilinx FPGA Vertix-7 achieving higher efficiency (frequency of operation/area) compared to the literature.

LUNCH (12:00–1:30)

THREADS

Thursday, March 20 / 1:30–3:10 pm / Ballroom A

Chair: **Yogendra Joshi**
DARPA MTO, Arlington, VA

Co-Chair: **Sharon Woodruff**
Booz Allen Hamilton, Washington DC

46.1: Direct Access Near-Junction Thermal Enhancement **(1:30)**

James Tweedie
MACOM, Durham, NC

46.2: Raytheon's Approach to Develop X-Band Multi-Finger >80 W/mm, T_{CH} < 225 °C Transistors **(1:50)**

Eduardo M. Chumbes, Matthew DeJarld, Ryan McGillicuddy, Cornelia Yang, Lovelace Soirez, Maher Tahhan
Raytheon, Andover, MA

Jeffrey Laroche
Raytheon, Tewksbury, MA

Scott Katzer, Virigina Wheeler, Brian Downey, David Meyer, Tatayana Feygelson, Karl Hobart
U.S. Naval Research Laboratory, Washington, DC

Debdeep Jena, Grace Xing, Zhiting Tian
Cornell University, Ithaca, NY

Srabanti Chowdhury
Stanford University, Stanford, CA

Nicholas Miller
Michigan State University, East Lansing, MI

Samuel Graham
University of Maryland, College Park, MD

Sukwon Choi
Penn State University, University Park, PA

46.3: Nano-structured Electrothermal Engineered Superlattice Device for CoLossal PowEr DenSity (NEEDLES): Polycrystalline Diamond (PCD) Integration Reduced Channel Temperature **(2:10)**

Shamima Afroz, Brian Novak, Michael Stocker, Brian Bersch, Patrick Shea, Sara Taylor, Vivian Ryan, Robert S. Howell
Northrop Grumman Mission Systems, Linthicum, MD

Srabanti Chowdhury, Mohamadali Malakoutian, Jeongkyu Kim
Stanford University, Stanford, CA

46.4: Pushing the GaN HEMT Technology Toward the Theoretical RF Power Limit **(2:30)**

Deep C. Dumka, Gergana Drandova, Brent Crittenden, Soufiane Karrakchou, Lidia El-Bouanani, Jinqiao Xie, Jose L. Jimenez, Jeffrey Krotosky
Qorvo, Inc., Richardson, TX

Ethan Scott, Patrick Hopkins
University of Virginia, Charlottesville, VA

Henry Aller, Emils Jurcik, Samuel Graham
University of Maryland, College Park, MD

Zeina Abdallah, Pharyanshu Kachhawa, Martin Kuball
University of Bristol, Bristol, UK

Marko Tadjer, Tatyana Feyelson, Daniel Pennachio, Bradford Pate, Jonathan Levine-Miles
U.S. Naval Research Laboratory, Washington, DC

Anna Kasperovich, Srabanti Chowdhury
Stanford University, Stanford, CA

This paper describes a combination of design, process and characterization of X-band Gallium Nitride HEMT to reduce its thermal resistance to below one sixth of the current standard GaN-on-SiC HEMT in production. Such an improvement is estimated to enable device operation at channel temperatures within a reliable regime while extracting over four times higher RF output power compared to the current standard. Target device is 1-mil thick GaN-on-SiC HEMT permanently bonded to a high thermal conductivity polycrystalline diamond substrate. Also, modified GaN epi-structure and device geometries are used to reduce the intrinsic and extrinsic thermal resistances.

46.5: Towards Thermal Resistance Improvement in High Output Power X-band GaN HEMTs **(2:50)**

Isaac Wildeson, Bill Zivasatienraj, Puneet Srivastava, Wen Zhu, Louis Mt. Pleasant, David Brown, Ken Chu
BAE Systems Inc, Nashua, NH

Craig McGray, Sean O'Leary, Robert Henry
Modern Microsystems, Inc., Gaithersburg, MD

Sukwon Choi, Seokjun Kim, Daniel Shoemaker, Husam Walwil
Pennsylvania State University, University Park, PA

Srabanti Chowdhury, Kelly Woo, Mohamadali Malakoutian
Stanford University, Stanford, CA

Patrick Fay, Yu-En Jeng
University of Notre Dame, Notre Dame, IN

Kyeongjae Cho, Youhwan Jo
University of Texas at Dallas, Dallas, TX

BREAK **(3:10–3:30)**

HOTS I

Thursday, March 20 / 1:30–3:10 pm / Ballroom B

Chair: **Todd Bauer**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Kwok-Keung Law**
DARPA, Arlington, VA

47.1: Development of GaN Transistor and SiC Transducer for High Temperature Pressure Sensing **(1:30)**

Ajay Kumar Visvkarma, John Micheal Gilroy, Yi-Shuo Huang, Jesse T. Kemmerling, Rongming Chu
Pennsylvania State University, University Park, PA

Ziyu Jiao, Shihan Liu, Hong Tang
Yale University, New Haven, CT

This paper reports recent development of GaN transistor and SiC transducer towards forming an integrated pressure sensor operating at high temperatures. The fabricated GaN FETs successfully showed the transistor operation up to 800 °C, with a current on/off ratio of 100. Major issues limiting the transistor performance at 800 °C includes degradation of ohmic contacts and increase of isolation leakage. The fabrication process for a SiC transducer is also developed, which features a thin membrane to achieve high sensitivity and partial-pressure N_2 backfilling for stable high-temperature operation. This transistor will be integrated to the transducer system to realize 800 °C pressure sensing in air ambient.

47.2: Integrated Sensors at High-Temperature Using Transferred Piezoelectric Transducers and Epitaxial Transistors **(1:50)**

Mark S. Goorsky, Lezli Matto, Eugene Kwon, Nishanth Ravi
University of California Los Angeles, Los Angeles, CA

Srabanti Chowdhury, Mahila Noshin, Hadi Sena, Matti Lawson Thurston
Stanford University, Stanford, CA

Neal Hall, Xiaoyu Niu, Ruochen Lu, Vakhtang Chulukhadze
University of Texas at Austin, Austin, TX

47.3: Towards an 800 °C Operational Temperature Piezoelectric Dynamic Pressure Sensor **(2:10)**

Mark Sheplak, Roozbeh Tabrizian, Philip X.-L. Feng
University of Florida, Gainesville, FL

Philip G. Neudeck
NASA Glenn Research Center, Cleveland, OH

Benoit R. Hamelin
EngeniusMicro, LLC, Atlanta, GA

Brian A. English
EngeniusMicro, LLC, Denver, CO

Accurate, high-bandwidth dynamic pressure measurements at elevated temperatures are crucial for a variety of applications such as hypersonic flight vehicle design, gas turbine operation, and geothermal energy exploration. Currently, there are no available sensor solutions for applications requiring a

bandwidth of 1 MHz with an operational temperature of 800 °C in air. Existing high-temperature, low-bandwidth silicon (Si)-based sensors are typically water-cooled or are remotely located using stand-off tubes enable the sensor to survive as Si becomes ductile 540 °C. Clearly, if operation above 500 °C is desired, a different material must be used for the diaphragm. This abstract presents the technology development required to realize a piezoelectric dynamic pressure sensor utilizing scandium-doped aluminum nitride (AlScN) on a silicon carbide (SiC) diaphragm that is capable of the required high-bandwidth performance at 800 °C in air. Modeling and sensor optimization methodologies are presented, along with materials optimization studies, fabrication and characterization approaches.

47.4: Hybrid Additive Manufacturing Printers to Accelerate Innovation in Severe Thermomechanical Environments **(2:30)**

Oliver Moreno, Benoit Hamelin
EngeniusMicro, Atlanta, GA

Bradley Marshall, Charles Rogers, Pat Gentile
EngeniusMicro, Huntsville, AL

Brian A. English
EngeniusMicro, Denver, CO

47.5: Reliable High Temperature Environment Pressure Detector (RHED) Through Advanced Integration of SiC and Piezoelectric Technologies **(2:50)**

Amrita Masurkar, Eric Langlois, Zachary Hileman, Isaac Wildeson, Jerry Li, Louis Lanzerotti, Daniela Torres
BAE Systems, Inc., Nashua, NH

Joshua Fox, Robert Lavelle, David Snyder
Pennsylvania State University, State College, PA

Shubham Prabhakar, Mariam Gigauri, Meera Garud, Noah Opondo, Siddharth Bhatnagar, Joseph Jewell, Dana Weinstein
Purdue University, West Lafayette, IN

Kushal Bhattacharjee
Kampanics, LLC, Kernersville, NC

BREAK **(3:10–3:30)**

POWER AMPLIFIERS I

Thursday, March 20 / 1:30–3:10 pm / Ballroom C

Chair: **Thomas Dalrymple**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Gregg Jessen**
MACOM Technology Solutions, Lowell, MA

48.1: A 24-to-29 GHz Compact Transmit/Receive Front-end Module Featuring an Asymmetric Doherty Power Amplifier and 0.22 mm² Area (1:30)

Xiaohan Zhang, Eric Wang, Qiang Zhou, Hao Guo, Taiyun Chi
Rice University, Houston, TX

We report a compact 24-to-29 GHz front-end module (FEM) in GlobalFoundries 22FDX process, featuring (1) a two-way asymmetric Doherty PA and (2) its co-design with LNA input matching and T/R switch. Compared with state-of-the-art 28 GHz FEMs, it demonstrates the highest OP1dB (19.6–20.6 dBm), the highest PAE at OP_{1dB} (25.0%–27.7%), the highest PAE at 9.5 dB back-off (14.2%–19.8%), the highest PAE_{avg} (18.6%) and a significant PAE_{avg} enhancement of 1.5× in 5G NR tests, a competitive NF (3.1–4.0 dB), and the smallest core area (0.22 mm^2).

48.2: Sensors for III-V Power Amplifier Self-Test (1:50)

Grace Gomez, Taylor Barton
University of Colorado Boulder, Boulder, CO

This paper presents temperature and impedance sensors for integration onto III-V power amplifiers (PAs) for self-test. Two impedance sensing techniques are described: a digital computation implementation and an all-analog VSWR sensor. The sensors' use-cases are compared based on circuit complexity and digital processing availability. A proportional to absolute temperature (PTAT) sensor is also presented. The sensor is based on a known ratio of currents and removes the need for characterization of the diode voltage-current relationship over temperature.

48.3: Multiple-Path Power Amplifier Architectures using a Modified Feedforward Technique (2:10)

Taylor Barton
University of Colorado Boulder, Boulder, CO

This paper presents an approach to power amplifier (PA) design that uses feedforward-like loop structures to modify the architecture's gain and distortion characteristics without sacrificing efficiency. In contrast to conventional feedforward amplifiers, the error or auxiliary amplifier also contributes to fundamental-frequency signal power. Two example architectures derived from this overall approach are summarized including with measured results.

48.4: A Ka-Band Reconfigurable Output Power PA MMIC **(2:30)**

Charles F. Campbell
Qorvo, Inc., Richardson, TX

The design and experimental results for a 4-level GaAs Ka-band output power reconfigurable amplifier MMIC is presented. The PA delivers up to 1.0 W of CW power when set to the maximum power mode. The MMIC can be electronically reconfigured for output powers of 1.0 W, 0.75 W, 0.5 W and 0.25 W. The small gain and return loss over the 17.3–20.2 GHz design band is typically 18 dB and less than –10 dB, respectively. The power added efficiency exceeds 30% for all 4 power settings and the AM/AM and AM/PM characteristics track between the power levels. The output power is reconfigured via three 0 V/-4 V control lines without any adjustment of the drain voltage supply.

48.5: A 5 to 25 GHz Four-Way Power Combined Low Voltage Driver Amplifier Robust to Radiation, Temperature, Process and Aging **(2:50)**

Jesse Moody, Phil Oldiges, Stefan Lepkowski, Tyler Liebsch
Sandia National Laboratories, Albuquerque, NM

This work presents an ultra-compact and broadband power amplifier operating from 5 GHz to 25 GHz with a peak output power of 21.6 dBm. This work accomplishes this performance thanks to the combination of an ultra-broadband digital distribution network and a broad-band series power combining network. By avoiding any band limiting electromagnetic coupling networks until the critical last stage, this work accomplishes exceptional bandwidth in a compact size. Unlike previous works targeting high power, compact size and extremely broad bandwidth, this work accomplishes this performance without using high supply voltages. By avoiding the significant levels of voltage stacking used in prior art to accomplish similar performance levels, this design drastically improves PVT robustness. Finally, this device is characterized for satellite communication use, showing robustness to aging, temperature and radiation through Total Ionizing Dose characterization.

BREAK **(3:10–3:30)**

Session 49 **(TA10 – Trusted, Assured and Cyber-secure Microelectronics)**

ARTIFICIAL INTELLIGENCE AND MACHINE LEARNING

Thursday, March 20 / 1:30–3:10 pm / Ballroom D&E

Chair: **Shawn Fetterolf**
Intel, Santa Clara, CA

Co-Chair: **Robert Freeman**
Synopsys, Inc., Sunnyvale, CA

49.1: BOMx: A Scalable Multi-Layered Solution with Computer Vision and Machine Learning for Assuring Electronics Supply Chain **(1:30)**

Tashfique Hasnine Choudhury, Beau Bakken
Caspia Technologies, Gainesville, FL

Pauline Paki
Science and Technology Directorate, Department of Homeland Security Washington, DC

49.2: AssertGen: Towards Secure Assertion Generation using Large Language Models **(1:50)**

Anand Menon, Samit Shahnawaz Miftah, Amisha Srivastava, Kanad Basu
University of Texas at Dallas, Richardson, TX

Assertions are critical components used in hardware verification, offering diverse features essential for facilitating functional verification. Traditional hardware assertion generation methods are not automated and require manual effort, leading to prolonged development cycles. Recent studies have demonstrated the potential of commercial Large Language Models (LLMs) in generating assertions by leveraging extensive textual data from design specifications. However, reliance on proprietary models such as GPT-4 compromises IP privacy and data confidentiality, impeding transparency and accountability. In this paper, we address the issue of generating hardware assertions by proposing an approach, AssertGen, to enhance the feasibility of open-source LLMs. Additionally, we employ Retrieval Augmentation Generation to refine these models further, mitigating hallucinations and errors. AssertGen demonstrates significant improvements, achieving up to a 44% increase in rouge-1 score, a 49% improvement in cosine similarity, and a 43.4% reduction in word error rate compared to state-of-the-art open-source models.

49.3: Honest to a Fault: Root-Causing Fault Attacks with Pre-Silicon RISC Pipeline Characterization **(2:10)**

Arsalan Ali Malik, Harshvadan Mihir, Aydin Aysu
North Carolina State University, Raleigh, NC

Fault injection attacks represent a class of threats that can compromise embedded systems across multiple layers of abstraction, such as system software, instruction set architecture, microarchitecture, and physical implementation. Early detection of these vulnerabilities and understanding their root causes along with their propagation from the physical layer to the system software is critical to secure the cyberinfrastructure. This present presents a comprehensive methodology for conducting controlled fault injection attacks at the pre-silicon level and an analysis of the underlying system for root-causing behavior. As the driving application, we use the clock glitch attacks in AI/ML applications for critical misclassification. Our study aims to characterize and diagnose the impact of faults within the RISC-V instruction set and pipeline stages while tracing fault propagation from the circuit level to the AI/ML application software. This analysis resulted in discovering a novel vulnerability through controlled clock glitch parameters, specifically targeting the RISC-V decode stage.

49.4: Large Language Models for Secure Microelectronics: Challenges and Opportunities (2:30)

Md Tanvir Arafin
George Mason University, Fairfax, VA

The current generation of large language models (LLMs) has demonstrated tremendous success in traditional natural language processing tasks (NLP) such as text generation, translation, summarization, query response, reasoning, and named entity recognition. Interestingly, these NLP tasks can also provide robust circuit design and testing assistance via automated circuit/netlist generation, code generation for testing and verification, and binary decompilation. Hence, this paper surveys the current state of the application of large language models in critical microelectronics applications, such as design automation and supply-chain analysis, and the security aspects of such techniques.

49.5: Enhancing Hardware Security: Detecting Vulnerabilities in HDL Codes Using Fine-Tuned Large Language Model (2:50)

Dipayan Saha, Sujan Kumar Saha, Jingbo Zhou, Mark Tehranipoor, Farimah Farahmandi
University of Florida, Gainesville, FL

Hardware vulnerabilities that allow attackers to exploit security-critical resources have become a significant concern, particularly in system-on-chip (SoC) architectures. Detecting and mitigating these vulnerabilities early in the hardware design process, specially at the register-transfer level (RTL), is critical for ensuring security. Large language models (LLMs) can play a vital role in this process. However, traditional pre-trained LLMs lack the necessary hardware security knowledge. To address this, we fine-tune an open-source LLM using common weakness enumeration (CWE) information to enhance its security detection capabilities. Additionally, we fine-tune the model with a security-aware dataset comprising both vulnerable and secure hardware designs, allowing it to more precisely identify weaknesses and potential threats. By leveraging these task-specific datasets, our fine-tuned LLM overcomes the limitations of traditional models. The results demonstrate that the fine-tuned LLM achieves higher accuracy in identifying security vulnerabilities, significantly reducing manual effort and improving security assurance in hardware development.

BREAK (3:10–3:30)

CHARACTERIZATION – ADVANCES IN MATERIALS

Thursday, March 20 / 1:30–3:10 pm / Ballroom H

Chair: **David Meyer**
Naval Research Laboratory, Washington, DC

Co-Chair: **Andrew Green**
Air Force Research Laboratory, Wright-Patterson AFB, OH

50.1: Complex Permittivities of Ultra-Low-Loss High-Purity Semi-Insulating 4H SiC at Different Millimeter-Wave Frequencies, Temperatures and Humidities (1:30)

Tianze Li, Lei Li, James C. M. Hwang
Cornell University, Ithaca, NY

High-purity semi-insulating (HPSI) 4H SiC has important high-frequency, high-power, and high-temperature applications. The applications require accurate knowledge of both ordinary and extraordinary permittivities, perpendicular and parallel, respectively, to the c axis of these semiconductors. However, due to challenges for suitable test setups and precision high-frequency measurements, little reliable data exists especially at millimeter-wave frequencies. This paper reports both ordinary and extraordinary permittivities of HPSI 4H SiC from 55 to 330 GHz, and their temperature and humidity dependence enabled by improving the measurement precision to two decimal points. The loss tangent, less than 1×10^{-4} over most millimeter-wave frequencies, is significantly lower than that of sapphire, our previous low-loss standard. Finally, both ordinary and extraordinary permittivities have weak temperature coefficients on the order of 10^{-4} per deg C. The knowledge reported here is especially critical to not only solid-state devices and circuits, but also windows for high-power vacuum electronics.

50.2: Electrical Characterization of GaN-on-Ga_2O_3 Bonded Vertical Schottky Diodes (1:50)

Stefan Kosanovic, Oguz Odabasi, Rijo Baby, Elaheh Ahmadi
University of California, Los Angeles, Los Angeles, CA

Xin Zhai
University of Michigan, Ann Arbor, MI

Kamruzzaman Khan, Boyu Wang, Umesh Mishra
University of California, Santa Barbara, Santa Barbara, CA

Bonded vertical GaN-on-Ga_2O_3 Schottky diodes with an ALD ZnO interlayer have been fabricated and characterized using temperature-dependent IV measurements. 5 nm ZnO shows the best temperature stability, I_{on}/I_{off} ratio, and highest current density, likely due to reduced $ZnGa_2O_4$ barrier at the bonded interface. A current density of ~2 kA/cm^2 was observed, as well as an I_{on}/I_{off} ratio of ~10^4.

50.3: High-Temperature Dielectric Characterization and Modeling at mmWave Frequencies (2:10)

Callen Macphee, Bahram Jalali
University of California, Los Angeles, Los Angeles, CA

Zane Cohick, Cesar Nieves Sanabria
Air Force Research Laboratory, Albuquerque, NM

Michael McCaffrey, David Casale, Aaron Buck, Young-Kai Chen
Coherent Aerospace and Defense, Philadelphia, PA

This study addresses the growing demand for RF sensing and communication devices capable of operating in extreme environments, such as those encountered in space exploration and industrial plasma processing. We present a robust methodology for measuring and modeling the complex permittivity of advanced dielectric materials at high temperatures (up to 1000 °C) and millimeter-wave frequencies (Ku, Ka, and W bands). Three materials—silicon carbide (SiC), lithium niobate (LiNbO3), and MLA433 ceramic—were characterized using both free space and waveguide measurement approaches, with careful consideration given to temperature compensation and thermal expansion effects. These findings were incorporated into a Python-based analysis tool and a COMSOL Multiphysics^{TM} material library, providing a versatile platform for rapid assessment and qualification of materials for advanced RF applications. This work establishes a robust framework for material characterization in harsh conditions, potentially accelerating the development of high-temperature, high-frequency electronic components for extreme environments.

50.4: Granular Metal Optimization for ns-Responsive Arresters (2:30)

Laura Biedermann, Michael McGarry, Simeon Gilbert, Tyler Bowman, Brianna Klein, Paul Kotula, Michael Siegal
Sandia National Laboratories, Albuquerque, NM

Nanosecond (ns) transient overvoltages threaten electrical grid stability. Equipment vulnerable to these common ns transients includes power electronics which integrate distributed energy resources (e.g. solar and wind generation) to the electrical grid. No grid-scale, self-breaking protection against ns transient overvoltages exists today. We are developing new arresters that shunt ns transients to ground. Such ns-responsive arresters will need materials with high E-field strength, high thermal stability, and high-pass filter performance. Granular metals (GMs), a type of disordered material, offer the desired filter response. To shunt grid-scale ns transients, we developed Mo-SiNx GMs having refractory-metal Mo nanoparticles in a high E-field strength silicon nitride matrix

50.5: Low Heat Fabrication of Metallic Interconnects (2:50)

Andrew Martin, Martin Thuo
NC State University, Raleigh, NC

BREAK (3:10–3:30)

HOTS II

Thursday, March 20 / 3:30–5:10 pm / Ballroom B

Chair: **Todd Bauer**
Sandia National Laboratories, Albuquerque, NM

Co-Chair: **Kwok-Keung Law**
DARPA, Arlington, VA

51.1: **Low SWaP, High Sensitivity, Multiferroic Strain-Modulated Magnetometers for Operation up to 500 °C** **(3:30)**

Sydney Acosta, Jonathan Tan, Michael D'Agati, Yujia Huo, Xuan Wang, Zekun Li, Mark Allen, Roy H. Olsson III
University of Pennsylvania, Philadelphia, PA

Thomas Mion, Peter Finkel, Konrad Bussmann, Margo Staruch
U.S. Naval Research Laboratory, Material Science and Technology Division, Washington, DC

51.2: **Temperature Dependence of DC and Small-Signal RF Parameters in 140 nm T-gate AlGaN/GaN HEMTs with Regrown Source/Drain Contacts** **(3:55)**

Biddut K. Sarker, Nicholas P. Sepelak, Karen Nishimura
KBR, Inc., Beavercreek, OH

Dennis E. Walker Jr., Antonio Crespo, Gary Hughes, Andrew J. Green, Ahmad E. Islam
Air Force Research Laboratory, Wright-Patterson AFB, OH

We conducted DC and small-signal RF characterization on AlGaN/GaN high-electron-mobility transistors (HEMTs) across a range of temperatures to analyze temperature-dependent variations in key device performance metrics including transconductance (g_m), extrinsic cutoff frequency (f_T), maximum gain frequency (f_{max}), unilateral power gain (UPG), and maximum stable gain (MSG). Our findings indicate that RF performance parameters decline with increasing temperature at a distinct rate. Specifically, for every 100 °C increase in temperature, f_T, f_{max} and MSG decrease by 8 GHz, 17 GHz, and 1 dB, respectively. We discovered that these performance changes are intrinsic to the device physics, independent of its geometry and operational mode.

51.3: Towards Monolithic Integration of AlN Transducers on AlN Substrates with High Electron Mobility Transistors **(4:20)**

Troy Tharpe, Travis R. Young, Andrew A. Allerman, Andrew I. Young, Jeffrey Kronz, Brianna A. Klein, Giovanni Esteves
Sandia National Laboratories, Albuquerque, NM

Alfred Zhao, Dhiren K. Pradhan, Roy H. Olsson III
University of Pennsylvania, Philadelphia, PA

Modern silicon-based sensors and electronics are unable to withstand the harsh, high-temperature environments demanded by aerospace, gas turbine, and geothermal applications due bulky and inefficient temperature mitigation approaches. Presented in this paper is a monolithic platform using aluminum nitride (AlN) transducers fabricated following an AlGaN high electron mobility transistor (HEMT) compatible process, capable of sensing a dynamic pressure field at high operational temperatures. Single crystal AlN provides low energy loss and high thermal stability, while doping these films with scandium (Sc) yields sputtered $Al_xSc_{1-x}N$ films with larger piezoelectric coupling and enhanced application sensitivity. To leverage both qualities, we demonstrate two approaches to $Al_xSc_{1-x}N$ deposition, metal organic chemical vapor deposited (MOCVD) AlN on tungsten (W) and sputtered $Al_{0.64}Sc_{0.36}N$ on W. We further use a single crystal AlN through-substrate etch to realize released, AlN and $Al_{0.64}Sc_{0.36}N$ pressure sensors with an expected flat band sensitivity up to 2.27 μV/Pa and bandwidth up to 1.11 MHz.

51.4: Single-Chip Pressure Transducer on a Thermally Hardened Heterogeneous SiC/JFET:GaN/HEMT Platform [SPOTS] **(4:45)**

Jacob Kupernik, A. Matthew Francis
Ozark Integrated Circuits, Fayetteville, AR

Jeffrey LaRoche, John Logan
Raytheon, Andover, MA

Caroline Reilly
Raytheon Technologies Research Center, East Hartford, CT

Stacey Kennerly
General Electric Research, Niskayuna, NY

David Mills, Austin Vera
Interdisciplinary Consulting Corp. (IC2), Gainesville, FL

Andrew Koehler
Naval Research Laboratories, Washington, DC

Philip Neudeck
National Aeronautics and Space Administration, Cleveland, OH

POWER AMPLIFIERS II

Thursday, March 20 / 3:30–5:10 pm / Ballroom C

Chair: **Tony Quach**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Farooq Amin**
Northrop Grumman, Morrisville, NC

52.1: Load Modulated Balanced Amplifier Enhanced by Quasi-Load-Insensitive Class-E Mode towards Minimal Thermal Dissipation for Dense Arrays (3:30)

Niteesh B. Vangipurapu, Jiachen Guo, Pingzhu Gong, Kenle Chen
University of Central Florida, Orlando, FL

This paper presents the first-ever hybrid asymmetrical load-modulated balanced amplifier (H-ALMBA) with an unprecedented efficiency enhancement by incorporating quasi-load insensitive (QLI) Class-E mode. It is revealed that the QLI Class-E can sustain the high efficiency throughout the back-off range during load modulation. As a proof-of-concept, an H-ALMBA prototype with a realistic transmission-line-based QLI Class-E carrier amplifier is developed using commercial GaN devices and branch-line couplers at 1.8 GHz. The experimental results with continuous-wave (CW) excitation well validates the envisioned performance with >80% efficiency achieved from 10-dB output back-off (OBO) to peak power. Moreover, the modulated measurement carried out with a 20-MHz-bandwidth 64-QAM OFDM signal 5G NR signal (PAPR >11-dB) demonstrates the highest-ever average efficiency up to 80%. This work promises minimal heat dissipation of PAs, enabling their integration into large and dense arrays that are crucial in many civilian and defense applications.

52.2: Scaling the Load Modulated Balanced Amplifier to MMIC Operation (3:50)

Yaqub Mahsud, Taylor Barton
University of Colorado Boulder, Boulder, CO

This work presents an evaluation of the load modulated balanced amplifier (LMBA) architecture using a balanced GaN MMIC power amplifier (PA) operating over 6–12 GHz. The balanced amplifier (BA) is characterized under CW excitation with over 30% drain efficiency over the octave band. To better understand the design space of the LMBA architecture, the isolated port of the output coupler of the balanced PA is then driven using an external control signal. Baseline balanced amplifier performance is then compared to overall drain efficiency for different assumed control signal PA efficiencies. The trade-offs between assumed control PA efficiency, control power, and overall efficiency are also presented.

52.3: Wideband Load-Modulated Double Balanced Amplifier (LMDBA) with Intrinsic Antenna Isolation for Active-Array-based Systems (4:10)

Jiachen Guo, Pingzhu Gong, Kenle Chen
University of Central Florida, Orlando, FL

This paper presents the first-ever wideband load-modulated double balanced amplifier (LMDBA) architecture with an intrinsic isolation to load. Building upon the foundational concept of the generic LMBA, by setting the control amplifier (CA) to balanced topology, the LMDBA can inherit the load-mismatch tolerance of balanced amplifiers. To demonstrate the principle, a wideband RF-input LMDBA is developed using GaN devices and commercial branch-line quadrature hybrid couplers from 1.9–2.7 GHz. The experimental results exhibit an efficiency of 54–75% at peak power and 45–60% at 10-dB output back-off under the matched condition of load. An efficiency up to 70.2% at peak power and up to 54.2% at 10-dB OBO is measured under 2:1 VSWR of load. Additionally, the PA's linearity profiles (AMAM and AMPM) can be well maintained against load mismatch. In modulated measurement, the efficiency and linearity performance can also be well maintained under various load mismatch.

52.4: 2–20 GHz Watt-Level Broadband PA Using Stacked Topology in HRL's 40 nm GaN HEMTs (4:30)

Clint Sweeney, Donald Y.C. Lie
Texas Tech University, Lubbock, TX

Jerry Lopez
NoiseFigure Research Inc. and Texas Tech University, Lubbock, TX

52.5: 0.13 µm SiGe Fully Integrated 28 GHz BPSK Transmitter with Directional Security (4:50)

Subhan Zakir, Waleed Ahmad, Ebrahim M. Al Seragi, Alireza Kiyaei, Atif H. Shah, Saeed Zeinolabedinzadeh
Arizona State University, Tempe, AZ

In this work, we have proposed a Binary-phase-shift keying (BPSK) transmitter (TX) with a built-in directional security feature. The proposed transmit scheme provides spatial security in the desired direction and constellation distortion in the other directions. The proposed TX is 2D scalable and is custom-designed, implemented on a 130 nm SiGe BiCMOS technology, and operates at 28 GHz. The proposed TX consists of a driver amplifier (DA), a phase shifter (PS), and two power amplifiers (PA) connected to the differential outputs of the phase shifter. The binary phase shift keying (BPSK) modulation is performed by switching the PAs ON and OFF. The TX demonstrates a gain of 22 dB, P_{1dB}, and P_{sat} output power of 6.13 dBm and 10.2 dBm respectively at 28 GHz.

CRYPTOGRAPHY ADVANCEMENTS AND CHALLENGES

Thursday, March 20 / 3:30–5:10 pm / Ballroom D&E

Chair: **Adam Waite**
Battelle Memorial Institute, Beavercreek, OH

Co-Chair: **Matthew Casto**
Midwest Microelectronics Consortium, Beavercreek, OH

53.1: Side-Channel Vulnerabilities in the FPGA Implementations of Lattice-Based Post-Quantum Cryptographic Schemes (3:30)

Yiting Wang, Zelin Lu, Gang Qu
University of Maryland, College Park, MD

Md Tanvir Arafin
George Mason University, Fairfax, VA

Lattice-based cryptography is the most popular construction for post-quantum cryptography. As the fundamental subblock of lattice-based cryptography, Number Theoretic Transform (NTT) is vulnerable regarding side-channel security and may leak secret information during its execution. This study explores the side-channel resistance of NTT implementation on field programmable gate arrays (FPGAs). To reveal the input of NTT, we deployed belief propagation, a probabilistic graphical model technique, using the power measurement from the NTT implementation on the CW305 Artix board.

53.2: A Co-Design Framework for Accelerating ASCON on RISC-V Embedded Systems (3:50)

Eslam Tawfik, Islam Elsadek
The Ohio State University, Columbus, OH

Cryptography is an essential component in every device, however, existing standards like AES and SHA are computationally expensive for resource-constrained IoT devices. To overcome this, NIST selected ASCON as a new LWC selected standard after an evaluation process that lasted over few years. This paper proposes a co-design framework that accelerates ASCON alongside a lightweight RISC-V processor to enhance encryption performance. Proposed approach is compared to implementing ASCON using a standalone processor. By accelerating ASCON permutations in hardware and integrating it into the Ibex RISC-V processor, efficient execution of various ASCON operations is enabled. operations including AEAD encryption/decryption, hashing, and extendable output functions. This design is fabricated using CMOS 22 technology. Hardware acceleration of permutations significantly boosted performance by 55x and 100x for AEAD and hashing, respectively, compared to SW. Additionally, it reduced energy consumption by 10.5x and 20x for AEAD and hashing, respectively.

53.3: FALCON STRIKE: Breaking the Emerging Post-Quantum Standard with a Side-Channel Attack **(4:10)**

Jinyi Qiu, Aydin Aysu
North Carolina State University, Raleigh, NC

53.4: True Random Number Generator with Theory-Backed Entropy Rates for ASICs **(4:30)**

Seth Cohen, Casey Fendley, Joel Bjornstad
Kratos SRE, Inc., Birmingham, AL

Cameron Musgrove
IERUS Technologies, Huntsville, AL

Nad Gilbert
Sandia National Laboratories, Albuquerque, NM

53.5: Using Cryptographically Assured Information Flow for Secure Remote Reprogramming **(4:50)**

Christian Femrite, Joshua Guttman, Moses Liskov
The MITRE Corporation, Bedford, MA

Secure Remote Reprogrammability is the ability to modify and install software on a physically distant device with confidence that known processes are executing their code on that device. This requires a hardware basis including cryptographic primitives. Cryptographically Assured Information Flow (CAIF) enables Secure Remote Reprogrammability through a simple mechanism. CAIF is akin to some operations in existing Trusted Execution Environments, but securely implements an ideal functionality defined in terms of logging and confidential escrow. We show how to achieve Secure Remote Reprogrammability for a wide variety of processes on a CAIF device using an FPGA-based prototype via cryptographically assured remote execution. Cryptographic protocol analysis demonstrates our security goals are achieved even against a strong adversary that may modify and execute unauthorized programs on the device. This capability is critical for long-lived devices amidst the quantum-resistant transition away from asymmetric digital signature algorithms and securing critical infrastructure and microelectronics supply chains.

RF TECHNOLOGIES FOR DIRECTED ENERGY

Thursday, March 20 / 3:30–5:10 pm / Ballroom H

Chair: **Gabriele Formicone**
Integra Technologies Inc., Phoenix, AZ

Co-Chair: **Tony Ivanov**
Army Research Laboratory, Adelphi, MD

54.1: High-Power, High-Frequency Gyrotron Development for Directed Energy Applications (3:30)

Monica Blank, Steve Cauffman, Kevin Felch
Microwave Power Products (MPP) (Formerly CPI), Palo Alto, CA

Philipp Borchard
Dymenso LLC, San Francisco, CA

Gyrotron oscillators, with their unmatched capabilities of producing large peak and average powers at frequencies from 15 GHz to 1 THz, are particularly well-suited to directed energy applications. Gyrotrons are currently under development for such varied directed energy applications as microwave thermal launch, microwave drilling, power transmission, and millimeter-wave imaging radar.

54.2: A 600 MHz Bandwidth 2.5 kW GaN/SiC Transistor Amplifier for Directed Energy at S-band (3:50)

Gabriele Formicone, William Veitschegger
Integra Technologies, Inc., El Segundo, CA

A single GaN/SiC transistor power amplifier with 2.5 kW peak power level and 600 MHz bandwidth for S-band Directed Energy systems is presented. The uniqueness of this solid-state power amplifier is based on the novel RF AlGaN/GaN on SiC transistors which can be operated at 150 V bias rather than standard 50 V. The 600 MHz bandwidth amplifier covers the frequency range of 1.9–2.5 GHz with a signal of 100 μs pulse width and 1% duty cycle. The paper discusses other possible improvements to further enhance bandwidth, peak power and / or pulse width and duty cycle.

54.3: GaN Based High-Power Microwave Phased Array Systems for Counter UAS Defense (4:10)

Lavanya Rau, Michael Hiatt, Jeff Logan, Matt Markel, Tyler Miller, Rebecca Menes
Epirus Inc., Torrance, CA

Gallium-Nitride (GaN) based High-Power Microwave (HPM) phased-arrays are a good fit for Counter Unmanned Aircraft System (C-UAS) defense, and in particular counter UAS swarms. Phased arrays offer the steering speed and beam width that can successfully engage multiple dispersed swarms. Use of Machine Learning (ML) techniques to finetune voltage to the GaN amplifiers enables long duration pulses and high duty cycles from high power-density devices. HPM backdoor access delivers a wider scope of effects that successfully end UAS mission.

54.4: Compact High Power Microwave Source for SWAP-limited Airborne Platforms **(4:30)**

Feyza Berber Halmen, Austin Stark, Christopher P. Ward
Missouri Institute for Defense & Energy, Kansas City, MO

Zachary B. Drikas, Bisrat D. Adissie, Victor M. Mendez, Matthew J. Dunlop-Gray
U.S. Naval Research Laboratory, Washington, DC

54.5: Antennas for Microwave-based Directed Energy **(4:50)**

Robert A. Koslover
SARA, Inc., Tyler, TX

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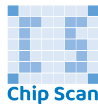

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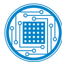

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