GOMACTech-23

Government Microcircuit Applications and Critical Technology Conference

PROGRAM

Microelectronics – the Engine to Keep the US Moving Forward

20–23 March 2023

Town and Country San Diego
San Diego, CA

www. gomactech.net

GOMACTech–2023
PROGRAM CONTENTS

WELCOME TO GOMACTECH-23

This year's conference is titled "Microelectronics – the Engine to Keep the US Moving Forward," and our robust technical program supports this theme with topics including Advanced Silicon-Based RF, Alternative Computing Paradigms, Counterfeit Detection and Avoidance, GaN Power Electronics, and much, much more.

The conference kicks off on Monday, 20 March, with our annual Trusted Suppliers Industry Day, created with the objective of promoting discussion among members of industry and government agencies that represent the interests of integrated-circuit and electronics producers who serve defense and aerospace applications. We have seen tremendous change since last year's Industry Day, not only with the enactment and funding of the CHIPS and Science Act but also with the increasing uncertainty regarding China's intentions with Taiwan. To provide insight into these issues, Dr. Tai Ming Cheung, recipient of multiple DoD Minerva Research Initiative awards and director of the University of California Institute on Global Conflict and Cooperation (IGCC), is scheduled to deliver the keynote address on the emergence of the Chinese techno-security state. Monday also features four workshops/tutorials: Advanced GaN Modeling, JFAC Hardware Assurance, GEEGAH Fab Capabilities & PDK for Acoustoelectric Devices, and AKOUSTIS Fab Capabilities & PDK for AlN/ScAlN.

Our Monday programming will conclude with a reception on the resort's Flamingo Lawn, which is open to *all* registered attendees. Please join us!

GOMACTech-23 formally opens on Tuesday, 21 March, with an outstanding morning Plenary Session that includes the keynote address "3DHI and the Coming Inflection Point in Microelectronics Manufacture" by Dr. Mark Rosker, director of DARPA's Microsystems Technology Office. Rosker will be followed by Ezra Hall, senior director of Global Aerospace and Defense Business at GlobalFoundries, whose talk is titled "Aligning Defense Microelectronics Technologies with Industry Needs: Fueling U.S. Success."

The keynotes will be followed by the Jack S. Kilby Lecture Series, with presentations from Dr. Waleed Khalil, professor of electrical and computer engineering at Ohio State University and the ElectroScience Lab, who will speak on "Analog Hardware Security: What We Don't Know *Will* Hurt Us," Mark M. Tehranipoor, chair of the Department of Electrical and Computer Engineering (ECE) at the University of Florida, with a talk titled "Secure Silicon Development Lifecycle: Pre and Post CHIPS," and Krystal Puga, Lunar Mission Architect for the Space Systems Sector at Northrop Grumman Corp., with the presentation, "James Webb Space Telescope Development and Latest Discoveries."

This year, we are also hosting three panel discussions: "Chips and Science Act Impact to DoD," on Monday, 20 March; and "Sifting Through the Chaos: Are Best Practices Achievable?" and "Perspectives on Computational Methods for Radiation Hardness Qualification," on Wednesday, 22 March. Be sure to check our on-site signage and online program for additional events that may have been added closer to our conference date.

The plenary, technical, and topical sessions are the major venues for information exchange at the conference. Other opportunities for technical interaction are provided by the exhibits program, which includes major IC manufacturers and commercial vendors of devices, equipment, systems, and services for nearly every facet of the electronics business. The exhibition opens on Tuesday, 21 March, at noon, and runs through Wednesday, 22 March, at 4:00 pm. On Tuesday evening, all attendees can network in a relaxing atmosphere during the Exhibitors' Reception.

Wednesday evening features the Evening Social, held this year at the San Diego Zoo, one of the country's premier zoos. A buffet-style dinner will be included, and we will have the opportunity to meet some of the animals "up close and personal." This is a ticketed event with an attendance cap, so if you're planning on attending, buy your ticket before Wednesday.

On Thursday morning, 23 March, a poster session that includes our annual student poster competition will take place.

GOMACTech was established primarily to review developments in microcircuit applications for government systems. Established in 1968, the conference has focused on advances in systems being developed by the Department of Defense and other government agencies and has been used to announce major government microelectronics initiatives such as VHSIC and MIMIC, and to provide a forum for government reviews.

The GOMACTech Conference is an Unclassified, Export-Controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, a signed Non-Disclosure Statement will be required.

GOMACTech-23 provides a forum for discussing and demonstrating advanced microelectronics and microsystems that can provide the means to develop confidence in transformational, leap-ahead technologies, and capabilities. GOMACTech is the premier forum for reporting on government-funded microcircuit research and other research efforts that focus on the technology needs of government systems.

This year's technical program is a result of the hard work and enthusiasm of the GOMACTech-23 Technical Program Committee. The committee members discussed and collaborated on the topics and presentations. The quality of the conference reflects this comprehensive team effort. We hope that you find GOMACTech-23 enlightening, rewarding, and enjoyable experience. Thank you for your active participation.

Dr. Morgan Thoma
U.S. Army Research Laboratory
Defense Microelectronics CFT
General Chair

Luciano Boglione
Naval Research Laboratory
Technical Program Chair

REGISTRATION

All sessions at GOMACTech-23 will be held at the Town and Country Resort in San Diego, CA. Both check-in and on-site registration will take place in the foyer.

Conference check-in and on-site registration hours:

Monday, 20 March	– 7:00 am – 6:30 pm
Tuesday, 21 March	– 7:00 am – 5:00 pm
Wednesday, 22 March	– 7:45 am – 5:00 pm
Thursday, 23 March	– 8:00 am – 3:00 pm

SECURITY PROCEDURES

The GOMACTech Conference is an Unclassified, Export-Controlled event that requires participants to be US Citizens or legal U.S. Permanent Residents. All registrants must provide proof of US Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, a signed Non-Disclosure Statement will be required. Note that all NDAs must be completed and signed on-site.

You may prove US citizenship with any of the following:

- U.S. Passport
- Birth certificate AND valid government-issued photo ID
- Naturalization certificate AND valid government-issued photo ID

The following are **NOT** proof of citizenship:

- Voter registration card
- Driver's license

Additionally, a signed non-disclosure statement will be required. Note that all NDAs must be completed and signed on-site.

GOMACTech WORKSHOPS and TUTORIALS

Trusted Suppliers Industry Day

Monday, 20 March, 2023, 8:00 am – 5:00 pm
Town and Country Ballroom A

Sunday Night Reception, March 19, 2023, 6:00 – 8:00 pm
Town and Country Foyer

The 12th Trusted Supplier Industry Day will be an interactive event with an opportunity for all attendees to hear from key leaders and provide input on the critical issues facing our community. We have seen tremendous change since last year's Industry Day, not only with the enactment and funding of the CHIPS and Science Act but also with the increasing uncertainty regarding China's intentions with Taiwan. To provide insight into these issues, Dr. Tai Ming Cheung, recipient of multiple DoD Minerva Research Initiative awards and director of the University of California Institute on Global Conflict and Cooperation (IGCC), is scheduled to deliver the keynote address on the emergence of the Chinese techno-security state. The keynote will be followed by a panel comprising members of the Defense Microelectronics Cross Functional Team discussing current focus and initiatives. Confirmed speakers include Dr. Mike Fritze of the Potomac Institute for Policy Studies and a member of the CHIPS Industry Advisory Committee; Dr. Nick Martin, Director, Defense Microelectronics Activity; Dr. Matt Kay, Program Manager,

Trusted & Assured Microelectronics; Dr. Alison Smith, Program Lead, DoD Microelectronics Commons; Dr. Yadu Zambre, Chief Microelectronics Technology Officer, AFRL; Kirk Thompson, MITRE Engenuity's Semiconductor Alliance; Chris Peters, Executive Director, U.S. Partnership for Assured Electronics; and Chris Mitchell, Vice President – Government Relations, IPC. As you can see, we have a full day planned designed to provoke thoughtful conversations! Please join us on March 20th to add your voice to the discussion of the most critical electronics issues of the day.

Advanced GaN Modeling Workshop

Monday, 20 March, 2023, 8:00 am – 5:00 pm
Town and Country Ballroom B

This technical workshop will provide an overview of state-of-the-art advances in non-linear modeling of GaN HEMT high-frequency power devices. The focus will be on a new paradigm shifting framework to be used in next-generation GaN MMIC designs. The new framework is founded on a physics-based compact modeling core. This relatively new class of GaN models, in contrast to purely empirical compact models, such as the popular Chalmers-Angelov model, include model parameters and equations that are tied to the GaN-specific physical material and geometry parameters. Examples are the ASM-HEMT model and the MIT Virtual Source physics-based compact models. These models enable improved scalability of process parameters (beyond the conventional gate-width and number of fingers), more meaningful statistical analyses, and also allow extrapolation to operating domains outside of the extraction data set. The Air Force Research Laboratory (AFRL), in collaboration with a Qorvo-led team, is pursuing extension of these advanced core modeling capabilities to equip designers with the ability to predict aging and reliability at the initial design stage, along with the nominal performance optimization capability required of all useful non-linear GaN compact models.

This workshop will provide an overview of the exciting new GaN modeling framework that is being developed, built around a physics-based modeling core, with extensions that include: foundry process scaling, advanced charge-trapping treatments, and long-term aging and reliability estimations that will bring significant new capabilities and agility to future GaN-based circuit design processes. Opportunities for additional organizations to participate in a related "Design Challenge" and to have future access to the new modeling framework will also be discussed.

JFAC Hardware Assurance Workshop

Monday, 20 March, 2023, 8:00 am – 5:00 pm
Town and Country Ballroom C

The Joint Federated Assurance Center (JFAC) is a federation of Department of Defense (DoD) organizations that promote and enable Software and Hardware Assurance. JFAC member organizations and their technical service providers interact with program offices and their performers to provide software and hardware assurance expertise and support, to include vulnerability assessment, detection, analysis, and remediation services, as well as information about emerging microelectronics risks, software and hardware assessment tools, services, and best practices.

This workshop will serve to educate the DoD and National Security Innovation Base (NSIB) community on JFAC capabilities and how programs, in support of meeting their microelectronics assurance needs, can utilize JFAC.

GEEGAH Fab Capabilities & PDK for Acoustoelectric Devices Tutorial

More-Than-Moore using Piezoelectric CMOS-MEMS PDK

Monday, 20 March, 2023, 8:00 am – 12:00 pm
Town and Country Ballroom D

This session will provide an overview of Geegah's efforts in developing a general-purpose piezoelectric MEMS on CMOS process design kit. Piezoelectric devices require innovations in material science, device physics, fabrication, and integration of electronics. Geegah is developing the PDK to reduce the barrier for designers to realize highly capable microsystems that can simultaneously enable sensing, actuation, and computation, in a turnkey fashion. This session will introduce the myriad piezoelectric devices such as RF filters, BAW transducers, PMUTs, microphones, speakers, energy harvesters, etc. The need for CMOS integration will be illustrated by circuit models that minimize sensitivity-degrading parasitic circuit elements. The manufacturing process of the Geegah PDK will be covered and will be compared to various other PiezoMEMS processes available. Examples of existing Piezo/CMOS devices will be presented that include Geegah ultrasonic imagers, PMUTs, and filters. Guidance on using the future PDK for sample devices will be given as a mini-tutorial. We aim to provide training to attendees on how to design new devices and make complex systems out of standard building blocks from the nominal Piezo-MEMS PDK. This workshop will serve to educate the broader DoD, intelligence community, defense industrial base, and industry on PiezoMEMS capabilities and services at Geegah.

AKOUSTIS Fab Capabilities + PDK for AlN/ScAlN Tutorial

Learn to Design in the Akoustis XBAW Foundry: A Manufacturable, Compact, High-Performance BAW and MEMs Filter Technology from 10's of MHz through Ku Band

Monday, 20 March, 2023, 1:00 – 5:00 pm
Town and Country Ballroom D

Akoustis uses pioneering materials science and process technology to develop resonators and RF filters with improvements in size, bandwidth, operating frequency, and power required for next generation WiFi, 5G infrastructure, 5G mobile, and defense applications. Bulk acoustic wave (BAW) is the technology of choice for RF signal filtering in the range of 2–7 GHz because it enables compact high-performance filters, leading to smaller systems, improved design tradeoffs and lowered system cost. The high quality-factor (Q) of BAW resonators enables improved performance, lower passband loss, and steeper filter skirts. Under the DARPA COFFEE program, Akoustis is expanding its BAW technology through Ku band.

In this workshop, Akoustis will showcase the capability and performance of XBAW, a novel manufacturing process, capable of producing state-of-the-art BAW RF resonators and filters. Using this XBAW wafer manufacturing process and a variety of advanced high-quality piezoelectric materials including single crystal and high purity polycrystalline AlN and AlScN thin films, RF filter solutions are created to address needed improvements in bandwidth, operating frequency, and output power compared to incumbent BAW technology deployed today. In addition to BAW filters, Akoustis will present the capability of the XBAW wafer manufacturing platform to extend into the MHz frequency spectrum, demonstrating high-performance Micro-Electro-Mechanical (MEMS) resonators using various acoustic vibrational modes with improved AlN and AlScN piezo electric materials. Akoustis will present its XBAW Foundry services, including an overview of the technology and examples of designing filters using process design

kits (PDK) offered by Akoustis XBAW Foundry for realizing BAW and MEMs resonators and filters.

2023 GOMACTech Panel Discussions

Monday Night Panel Discussion

CHIPS and Science Act Impact to DoD

Monday, 20 March, 2023, 5:00 – 6:00 pm
Palms Ballroom 4-6

In August 2022, the CHIPS and Science Act became law. It was designed to bolster the US semiconductor supply chain and promote research and development of advanced technologies in the United States. There are a large number of efforts throughout the country to provide capabilities that DoD can take advantage of. It is important to sustain this investment by leveraging it for advanced research to enable DoD to achieve its desired goals.

This panel will provide a perspective from various organizations about the current state. The discussion points are: where organizations' efforts fit with respect to the CHIPS Act, a perspective on where DoD microelectronics technology needs are going, and how the CHIPS Act is influencing plans for the department. Also included will be comments on the positive impacts so far and the other opportunities that the CHIPS Act will be shaping.

Wednesday Morning Panel Discussion

Sifting Through the Chaos: Are Best Practices Achievable?

Wednesday, 22 March, 2023, 10:30 am – 12:10 pm
Palms Ballroom 4-6

There are many official and de facto standards that inform and prescribe approaches and methodologies for designing microelectronics in the marketplace today. With the Joint Federated Assurance Center (JFAC) putting forward a framework to ensure DoD microelectronic systems are appropriately scrutinized and assessed for assurance, there is a need to develop best practices that guide the community in implementing these requirements. Join us as we discuss the good, the bad, and the ugly of best practices and how they might be useful.

Wednesday Afternoon Panel Discussion

Perspectives on Computational Methods for Radiation Hardness Qualification

Wednesday, 22 March, 2023, 1:30 – 3:10 pm
Palms Ballroom 4-6

The emergence of Space as a warfighting domain as well as the explosive growth of the commercial space industry have led to an increase in demand for electronic systems capable of operating in high-radiation environments. The process of qualifying rad-hard components is time-consuming, expensive, and taxing on the nation's infrastructure of radiation sources and radiation testing facilities. Industry trends toward heterogeneous integration, 3D chip architectures, novel materials and interconnects, and the desire to employ commercial off-the-shelf (COTS) electronics in space applications exacerbate the problem. The constraints of the current US radiation test infrastructure motivate the need to augment existing test methodologies with novel computationally efficient methods to facilitate the qualification of state-of-the-art microelectronic systems for space applications.

The focus of this panel is to discuss the modeling and simulation approaches that are needed to augment traditional experimental qualification and the challenges facing their validation and eventual adoption. Representatives from government end users, academia, and commercial foundry and computational software vendors will offer their perspectives.

LUNCHES

Lunches will be provided near the exhibition in the Golden State Ballroom.

NETWORKING RECEPTION

Sunday 19 March 6:00 – 8:00 pm
Town and Country Foyer

We are pleased to hold a special get-together with the Trusted Supplier Industry Networking Reception on Sunday evening. Please join us for some food and drinks (2 drink tickets included), meet your industry friends and colleagues, and relax before Monday's full agenda begins.

All GOMACTech-23 registrants are invited to the Sunday evening Reception.

TUESDAY EVENING EXHIBITORS' RECEPTION

On Tuesday evening, an Exhibitors' Reception, where attendees can mix in a relaxing atmosphere with food and good spirits, will be held from 6:00 to 8:00 pm on the exhibit hall floor in the Golden State Ballroom.

WEDNESDAY EVENING SOCIAL

The Wednesday Evening Social will be held at the San Diego Zoo. A buffet-style dinner is included, as is a chance to meet some of the animals. Tickets will cost $50 for adults and $15 for children. Shuttle buses will leave the hotel for the 7:30 to 9:30 pm event starting at 6:30 p.m. This event may sell out, so be sure to purchase your tickets early. Note: when you register for the zoo event, your name will be added to a list that will allow you to board the bus for the zoo. Once at the zoo, you will receive your entrance ticket.

EXHIBITION

An exhibition made up of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are encouraged to visit the exhibition when they have some free time. The exhibition will be located in the Golden State Ballroom. Coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening, an Exhibitors' Reception, where attendees can mix in a relaxing atmosphere with food and good spirits, will be held from 6:00 to 8:00 pm.

Exhibition hours are as follows:

Tuesday, 21 March – 12:00 pm – 8:00 pm
Wednesday, 22 March – 9:00 am – 4:00 pm

List of Exhibitors

3D Glass Solutions, Inc.
Advanced Test Equipment Corp.
Alphacore, Inc.
Andes Technology Corp.
Astronics Test Systems
Avalanche Technology
BAE Systems
Battelle
Boeing
Bruker
C&D Semiconductor Services, Inc.
Cactus Materials, Inc.
Cadence
Caspia Technologies
Central Semiconductor Corp.
Checkpoint Technologies
Chip Scan, Inc.
Codasip
CoolCAD Electronics
Cryptography Research at Rambus
Cycuity
Defense Technical Information Center (DTIC)
DMEA TAPO
ENGIN-IC, Inc.
Evatec North America
Exodus Advanced Communications
Extreme Waves
Finetech USA
Flex Logix, Inc.
Frontgrade
GDSI
Globalfoundries U.S., Inc.
Golden Altos Corp.
Graf Research Corp.
HRL Laboratories LLC
IBM
Indiana Integrated Circuits LLC
Integra Technologies LLC
Intrinsic ID
Intrinsix Corp.
JEOL USA, Inc.
Jazz Semiconductor Trusted Foundry
Kansas City National Security Campus
Keyence Corp. of America
Keysight Technologies
Knowles Precision Devices
Linear Integrated Systems
Marvell Government Solutions
Menta eFPGA, Inc.
Mercury Systems
Metamagnetics
Microchip Technology, Inc.
Micropac
Microsanj
Micross Components
MIT Lincoln Laboratory
The MOSIS Service, ISI, USC
Nano OPS, Inc.
Nimbis Services, Inc.
Noble Metal Services
Northrop Grumman
NSTXL

onsemi
Otava
Ozark Integrated Circuits, Inc.
PacTech USA, Inc.
Palomar Technologies, Inc.
Penn State University Applied Research Laboratory
Photronics, Inc.
QML, Inc.
QP Technologies
Quantum Design International
QuickLogic Corp.
Raith America, Inc.
Raytheon Technologies Research Center
Real Intent
Riscure
Rochester Electronics LLC
Rogers Corp.
Siemens
Silicon Assurance
Silitronics Solutions, Inc.
SkyWater Technology
Spectial Design + Test, Inc.
Spirit Electronics
SRI International
StratEdge Corp.
Sumitomo Electric USA
Synopsys
Tektronix Component Solutions
Tenet 3 LLC
Top Talent Search Experts LLC
TopLine Corp.
Toppan Photomasks Round Rock, Inc.
Trusted Semiconductor Solutions, Inc.
University of California, Davis
Vistec Electron Beam
VORAGO Technologies
Wolfspeed
XTREME Semiconductor

GOMACTech–22 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech-22 will include the George Abraham Outstanding Paper Award, a Best Poster Paper Award, and a Best Student Poster Paper Award. Presentation of these well-deserved awards will take place during the Plenary Session on Tuesday morning in the Town and Country Ballroom. The GOMACTech-22 winners are as follows:

The George Abraham Outstanding Paper Award (12.2)

"High Density Power Electronics in Emerging Aerospace and Defense Applications"

Jeffrey Ewanchuk and Parag Kshirsagar
Raytheon Technologies Research Center

Best Poster Paper Award (P.41)

"GlobalFoundries Silicon Fabrication Assurance"

Raymond Goss, Dr Jeremy Muldavin, Sebastian Ventrone
GLOBALFOUNDRIES

Joy Angelle, Steve Walters, Don Wilczewski
Aerocyonics, Inc.

Research funded by OUSD(R&E)

The Les Palukti Best Student Poster Paper Award (P.12)

"On the Use of 3D Printing for Realization of L-band Arrays with Meanderline Polarizer"

Erik Lier, Tom Hand, Neill Kefauver, Songyi Yen,
Gaeron R. Friedrichs, Ljubodrag Boskovic, Isaiah Pisani,
Dejan Filipovic
University of Colorado Boulder

Erik Lier, Tom Hand, Neill Kefauver
Lockheed Martin Space Systems

RATING FORM / QUESTIONNAIRE

Don't forget to vote for your favorite presentation this year before you leave the conference. A rating form will be handed out to everyone at conference check-in. Note that those presenters that do not submit a paper for the CD or USB are not eligible to be voted on. Also, a short questionnaire will be handed out so that we can secure your feedback about the conference. To encourage submission of these forms, GOMACTech has a special gift for all attendees submitting both completed forms. Please turn your forms in at the conference registration desk when you leave the conference to receive your gift item. You can also complete these forms by using the GOMACTech mobile app. Please see the front desk for any assistance submitting your rating.

CD-ROM AND USB DIGEST

The GOMACTech CD-ROM and USB Digest, containing searchable, condensed versions of submitted papers presented at the conference, will be distributed to all registrants. Additional copies can be purchased at the conference for $40.00 per CD and $50.00 per USB. This publication is the only record of the conference. Previous GOMAC Digests will, upon request, be made available to qualified Defense Technical Information Center (DTIC) users. Visit the GOMACTech History page (www.gomactech.net/gomac_history.html) for instructions to request proceedings from prior conferences.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech-22 include: Department of Defense (Army, Navy, Air Force) ... National Aeronautics and Space Administration ... Department of Commerce (National Institute of Standards and Technology) ... National Security Agency ... Department of Energy (Sandia National Laboratories and National Nuclear Security Administration) ... Defense Logistics Agency ... Defense Threat Reduction Agency ... Defense Advanced Research Projects Agency ... National Reconnaissance Office ... Intelligence Advanced Research Projects Agency

GOMACTech WEB SITE

Information on GOMACTech may be obtained through its web site at www.gomactech.net.

CONFERENCE CONTACT

Anyone requiring additional information about GOMACTech should contact the Conference Coordinator:

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TUESDAY, 21 MARCH

PLENARY SESSION

Tuesday, 21 March / Town and Country ABCD Ballroom

Continental Breakfast **(7:00–8:30)**

Opening Remarks and Awards **(8:15–8:45)**

Morgan Thoma, GOMACTech 2023 Conference Chair

Keynote Address I **(8:45–9:30)**

Dr. Mark Rosker
Director
Microsystems Technology Office (MTO)
DARPA

"3DHI and the Coming Inflection Point in Microelectronics Manufacture"

Two kinds of scaling, geometric and economic, are both driving microelectronics to a critical inflection point. The future of microelectronics manufacture, critical for defense and commercial applications, will depend on the emerging technology of three-dimensional heterogeneous integration (3DHI). This talk will highlight DARPA's strategy, within the Electronics Resurgence Initiative 2.0 (ERI 2.0), to create a national capability for fabricating and prototyping next-generation 3DHI microsystems. Other key challenges within ERI 2.0 will also be presented.

Keynote Address II **(9:30–10:15)**

Ezra Hall
Senior Director
Global Aerospace and Defense Business
GlobalFoundries

"Aligning Defense Microelectronics Technologies with Industry Needs: Fueling US Success"

Microelectronics are pervasive in society, transforming the way we work and live, and are used across countless industrial, consumer, and defense applications. As the underpinning technologies have advanced to meet these growing and diverse application needs, today's business models must account for the design, development, and manufacturing of semiconductors to ensure a reliable and sustainable supply. With the nation's increased focus on domestic semiconductor production to address economic and national security, the need to align the needs of the US government and industry with dual-use technology roadmaps could not be more critical. In this talk, Hall will discuss the business and technical factors required to keep the US moving forward in this critical sector.

BREAK **(10:15–10:30)**

Jack S. Kilby Lecture Series **(10:30–12:00)**

Dr. Waleed Khalil
Professor
Electrical and Computer Engineering
Ohio State University and the ElectroScience Lab

"Analog Hardware Security: What We Don't Know* Will *Hurt Us"

Advances in microelectronics have had a tremendous positive impact on society, providing users with more features, more automation, and more connectivity. However, these advancements come at a cost, as increasing

complexities in designs and increased reliance on offshoring lead to growing threats and vulnerabilities. While there has been some research into hardware security in response to these vulnerabilities, most work has focused on the digital domain, as it is easier to see the circuit world that is abstracted into 1s and 0s. However, this abstraction leaves largely unaddressed the area of analog hardware security. This talk will provide some of the initial strides that the analog community has taken to augment its digital counterpart, building toward more secure and resilient hardware.

Mark M. Tehranipoor
Intel Charles E. Young Preeminence
Endowed Chair Professor
Chair of the Department of Electrical and
Computer Engineering (ECE)
University of Florida

"Secure Silicon Development Lifecycle: Pre and Post CHIPS"

The CHIPS Act has brought much needed excitement for onshoring the front-end and back-end fabrication test and facility. However, much of the security concerns during the design of modern system on chips (SoCs) or system-in-package (SiPs) have little to do with onshoring. This talk will discuss challenges to securing silicon development lifecycle with CHIPS in place, offer solutions to engineers and practitioners, and present research opportunities for academics.

Krystal Puga
Lunar Mission Architect
Space Systems Sector
Northrop Grumman Corporation

"James Webb Space Telescope Development and Latest Discoveries"

This lecture includes an overview of the James Webb Space Telescope Mission, incorporating key facts and a description of the development of the telescope, including assembly, integration, and test. The lecture will describe some of the technical challenges, breakthrough technologies, and logistics leading up to launch campaign. It will also address the science objectives and latest discoveries that have been published across many platforms.

LUNCH **(12:00–1:00)**
Golden State Ballroom

Session 1

ADVANCED SILICON-BASED RF

Tuesday, 21 March / 1:30 – 3:10 pm /
Town and Country Ballroom A

Chair: **James Wilson**
DARPA, Arlington, VA

Co-Chair: **Christopher Coen**
Georgia Tech Research Institute, Atlanta, GA

1.1: **45 nm PDSOI SiGe BiCMOS for mm-Wave Applications** **(1:30)**

Alvin Joseph, John Pekarik
GlobalFoundries, Essex Junction, Vermont

Vibhor Jain, Sudesh Saroop, Teng-Yin Lin
GlobalFoundries, Malta, NY

Venkat Vanukuru, Sharma Prateek Kumar, Santosh Gedela, Vaibhav Ruparelia
GlobalFoundries, Bangalore, India

1.2: **A 67 GHz 23 mW Receiver Utilizing Complementary Current Reuse Techniques** **(1:50)**

Jesse Moody, Stefan Lepkowski, Travis Forbes
Sandia National Labs, Albuquerque, NM

Millimeter wave frequencies enable area-efficient antennas and steerable arrays, but typically entail a significant power penalty degrading SWAP. Drastic power reduction combined with asymmetric communication links can enable extremely SWAP-efficient satellite links among other applications. This paper presents a very low power, low noise receiver operating at V-band which is enabled by the application of ultralow power RF design techniques in the mm-Wave domain. This device takes advantage of both complementary current reuse and moderate inversion biasing, combined with a compact and extremely power-efficient frequency doubler, to achieve 23 mW power consumption while operating between 60 GHz and 75 GHz for an RF bandwidth of 15 GHz.

1.3: **430-GHz Concurrent Transceiver Array in CMOS for Power-Efficient High-Resolution Stand-off Imaging** **(2:10)**

Wooyeol Choi
Oklahoma State University, Stillwater, OK

Yukun Zhu, Pranith R. Byreddy, Shenggang Dong, Kenneth K. O
University of Texas at Dallas, Richardson, TX

A 430-GHz 1 × 3 array of concurrent transceiver pixels is demonstrated in 65-nm CMOS. Each pixel comprises a 143-GHz differential oscillator, a single-balanced subharmonic mixer using a pair of diode-connected NMOS transistors, a differential patch antenna, and an IF LNA. The oscillator doubles as a third harmonic transmitter and an LO for the mixer to perform transmit/receive operations at the same time, like continuous-wave radars. The pixel occupies an area of 370 × 380 μm^2, which is close to half wavelength square at 430 GHz, making it suitable for uses in 2-D focal-plane arrays. The array exhibits a combined effective isotropic radiated power of −4 dBm at a DC power consumption of 85.8 mW. The DSB noise figure of individual pixel is 39 dB. The array is integrated with a 6-cm diameter Cassegrain antenna to perform stand-off imaging of targets at 3 m through heavy fog and a cardboard box with an angular resolution of ~0.7°.

1.4: A 0.35–3.4 GHz Fully Integrated Highly Reconfigurable Direct-Conversion Receiver **(2:30)**

Justine Saugen, Travis Forbes, Chelsi Weiland, Ian Sobering, Bo Lindstrom, Mitchell Powner
Sandia National Laboratories, Albuquerque, NM

Across the government space, RF receivers are needed with a variety of specifications across frequency, filtering, gain and more. Custom designed integrated circuits provide full customization, however, can come at a high cost with limited application space. In this work, we present a 0.35–3.4 GHz direct-conversion receiver with highly reconfigurable programming, employing 3 RF paths to cover the large RF bandwidth and 2 programmable baseband filters. The receiver fully integrated and implemented in a 180 nm SOI CMOS with die area 7 mm^2.

1.5: Wideband X/Ku/Ka SATCOM 8- and 16-Channel SiGe Transmit and Receive (Two Beams) Beamformer Chips with High Performance **(2:50)**

Gabriel Rebeiz
UCSD, La Jolla, CA

Wajih Elsallal
The MITRE Corporation, Bedford, MA

This paper presents a 5–33 GHz 8-channel transmit beamformer and 4–26 GHz 16-channel receive beamformer chips implemented in 90 nm SiGe BiCMOS HBT technology. The measured small-signal gain is 24–25 dB for both chips with 5-bit phase-shifter operation and >20 dB gain control. A peak OP1dB and OPsat of 13–14 dBm is achieved at Ku-band for the transmit chip, and a NF of <2.2 dB is achieved at 4–20 GHz for the Rx chip, which is a record for such a wideband design. Application areas are ground terminals capable of communications with X, Ku and Ka-band satellite systems.

BREAK supported by CADENCE **(3:10–3:30)**
Golden State Ballroom

Session 2

EO SENSING COMPONENTS & TECHNOLOGIES

Tuesday, 21 March / 1:30 – 3:10 pm /
Town and Country Ballroom B

Chair: **Ronald Rapp**
Air Force Research Laboratory, Eglin AFB, FL

Co-Chair: **Igor Anisimov**
Air Force Research Laboratory, Wright-Patterson AFB, OH

2.1: Photodetector Focal Plane Arrays Integrated with Silicon Micropyramidal Structures in MWIR (1:30)

Grant W. Bidney, Vasily N. Astratov
University of North Carolina at Charlotte, Charlotte, NC and
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

Joshua M. Duran, Gamini Ariyawansa, Igor Anisimov
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

Kenneth W. Allen
Georgia Institute of Technology, Atlanta, GA

Light-concentrating truncated Si micropyramidal arrays with 54.7° sidewall angles were successfully integrated with PtSi Schottky barrier photodetectors. Four different devices consisting of 10 × 10 photodetectors with 60 μm pitch combined in parallel were tested, where significant enhancement capability was demonstrated by the Si micropyramids. The device consisting of one hundred 22 μm square detectors monolithically integrated with the light-concentrating micropyramidal array displayed signal enhancement of up to 4 times compared to the same size 22 μm square photodetector device without the light concentrators.

2.2: Mid-Infrared Rainbow Light-Emitting Diodes (1:50)

Aaron J. Muhowski, Abhilasha Kamboj, Daniel Wasserman
University of Texas at Austin, Austin, TX

We present, both theoretically and experimentally, a guided-mode resonance light-emitting diode. Such a device closely integrates a waveguide and grating structure. The restriction of allowed propagating wavevectors and outcoupling provided by the grating produce a unique far-field emission spectrum—a strong, narrow, transverse-electric polarized peak shifts at a rate of 1.17 meV/° from 5.4 μm to 4.4 μm as the angle with respect to the surface normal is increased. For collection angles approaching 0°, we obtain linewidths of 2.4 meV. This class of devices may be useful in high spectral bandwidth, compact sensing applications requiring spectral discrimination.

2.3: Low-Power Intra-Scene High Dynamic Range ROIC for IR Applications **(2:10)**

Roman Fragasse, Ramy Tantawy, Megan Manifold, Shane Smith, Gary Sung, Josh Coffey, Ara Rexford
SenseICs Corporation, Columbus, OH

Suat Ay
Aynano Technology, LLC, Pullman, WA

Waleed Khalil
The Ohio State University, Columbus, OH

2.4: High-performance Electrically Reconfigurable Infrared Metasurfaces based on Phase-change Materials **(2:30)**

Kyung-Ah Son, Jeong-Sun Moon, Ryan Quarfoth, Hwa-Chang Seo, Chuong Dao, Elias Flores, Aaron Bluestone, Hanseung Lee, David Chow
HRL Laboratories, Malibu, CA

2.5: Curved Compact Infrared Imaging Array **(2:50)**

Christopher Kauffman
Northrop Grumman Mission Systems, Rolling Meadows, IL

Jeff Eisenhaure, Paul Tittel, Maria Rahaniotis, Paul Harms, Alex Toulouse
Northrop Grumman Mission Systems, Linthicum, MD

Jason Kulick, Carlos Ortega, Shakhriyar Azizov
Indiana Integrated Circuits (IIC), South Bend, IN

Robert Patti
NHanced Semiconductors Inc., Batavia, IL

Sangki Hong, Choukri Allali
NHanced Semiconductors Inc., Morrisville, NC

Stefan Lauxtermann, Per Olov Pettersson, Frank Behzadi
Sensor Creations Inc. (SCI), Camarillo, CA

BREAK supported by CADENCE **(3:10–3:30)**
Golden State Ballroom

Session 3

NATIONAL STRATEGY & STANDARDS

Tuesday, 21 March / 1:30 – 3:10 PM /
Town and Country Ballroom C

Chair: **Lisa McIlrath**
P&L Partners, LLC, Arlington, VA

3.1: **On Supporting National Security Needs: Intel's Perspective on Enabling a Commercial Business to Support National Security Needs** **(1:30)**

Shawn Fetterolf, Gena Gleason, Tyler Schmidt, Sean O'Neill
Intel Federal LLC, Fairfax, VA

3.2: **DoD Challenges in Leveraging Open Source Hardware to Accelerate Technology Development** **(1:50)**

Brendon Chetwynd, Kyle Ingols
MIT Lincoln Laboratory, Lexington, MA

Mark Labbato, Jeff Durrum, Kyle Ahearn, Tristan Hudson, Gokul Srinivasan, Christian Giesler
Booz Allen Hamilton, Beavercreek, OH

Saverio Fazzari
Booz Allen Hamilton, Arlington, VA

The Department of Defense (DoD) is looking to leverage advanced technologies across a wide range of domains and will continue to rely heavily on contractors. Independent verification and validation of the technology is critical to ensure relevance and correctness. Systems include all types of components including: COTS parts, Printed Circuit Boards (PCBs), Field Programmable Gate Arrays (FPGAs), and Custom Integrated Circuits (CICs). Often, FPGAs and CICs leverage third-party intellectual property (3PIP), which may have questionable provenance. In this paper, we explore the use of Open-Source Hardware (OSH) to mitigate some of these concerns and expand the DoD's available list of options. As a primary study, we leverage the Common Evaluation Platform (CEP), a moderately complex OSH System on Chip (SoC) platform capable of targeting FPGA and CICs. We explore some of the benefit and drawbacks of the OSH methodology including verification and sustainment, concluding with a recommended path forward.

3.3: **Obsolescence Mitigation and Modernization of Legacy DoD Microelectronics Systems** **(2:10)**

Jeffrey Durrum
Booz Allen Hamilton, Beavercreek, OH

P. Len Orlando III, Vipul J. Patel
Air Force Research Laboratory, Wright-Patterson AFB, OH

The DoD relies heavily on legacy systems that, in many cases, were designed, manufactured, and first implemented decades ago. These systems are even further outdated due to the extremely fast pace of microelectronics innovation. Many functions that were once performed on large circuit boards populated with discrete electronic components are now implemented on Application Specific Integrated Circuits (ASIC) or Systems on Chips (SoC). Such legacy systems present unacceptable Size, Weight, Power and Cost (SWap-C), require costly maintenance, and necessitate prohibitively difficult sourcing of antiquated components. In an effort to mitigate obsolescence and sourcing risks, modern microelectronics devices can be designed and fabricated to modernize legacy systems at advanced nodes. This paper presents the challenges to, and benefits of, implementing a legacy system on a state of the art SoC.

3.4: Benchmarking Cryptographic Engine for Upcoming NIST FIPS Standard LWC **(2:30)**

Eslam Yahya Tawfik, Islam Elsadek
The Ohio State University, Columbus, Ohio, OH

Doug Gardner, John Ross Wallrabenstein, Erik MacLean
Analog Devices, Wilmington, Massachusetts

Rosario Cammarota, Sohrab Aftabjahani
Intel Co., Santa Clara, California

IoT and resource-constrained environments necessities a new standard for cryptography. As current standards require demanding resources and energy consumption. Hence NIST has a standardization process for a LWC algorithm that shall fit in resource-constrained devices. The standardization process is concluding with 10 final candidates. The aim of this work is to benchmark the 10 candidates in a fair comparison using the same optimizations and architectures. The whole spectrum of designs and implementations (HW, HW/SW co-design and SW using a resource-constrained RISC-V processor) are designed and evaluated for all candidates. The designs are implemented and fabricated using CMOS GF22FDx technology. Results show HW implementation to enhance the throughput up to 99000× and energy efficiency up to 57000× compared to SW implementation. Moreover, Xoodyak and TinyJambu are the most energy efficient algorithms while Sparkle and Xoodyak are providing the highest throughput.

3.5: Procurement and Acquisition Landscape of Microelectronics Intellectual Properties within the Department of Defense: Experiences during the MASTER Task Order **(2:50)**

Mark Labbato, Ryan Walker, Dina Saah, Kyle Ahearn, Jeff Durrum, Rachael Kolker, Barry Vincent, Saverio Fazzari
Booz Allen Hamilton, Beavercreek, OH

Scott Wartenberg
Wartenberg Consulting, LLC, Vienna, VA

Matthew D. Sale, P. Len Orlando III, Kevin J. McCamey, Vipul J. Patel
Air Force Research Laboratory, Wright-Patterson AFB, OH

BREAK supported by CADENCE **(3:10–3:30)**
Golden State Ballroom

Session 4

GENERATING RF WITH PHOTONIC OSCILLATORS FOR LOW NOISE (GRYPHON)

Tuesday, 21 March / 1:30 – 3:10 pm /
Town and Country Ballroom D

Chair: **Gordon Keeler**
DARPA MTO, San Diego, CA

Co-Chair: **Justin Cohen**
Booz-Allen Hamilton, McLean, VA

4.1: **Generating RF with Photonic Oscillators for Low Noise (GRYPHON)** **(1:30)**

Gordon Keeler
Defense Advanced Research Projects Agency (DARPA)
Microsystems Technology Office, Arlington, VA

Justin Cohen
Booz Allen Hamilton, Arlington, VA

Photonic microwave generation translates high-stability signals from optical to microwave frequencies, and forms the basis for the world's lowest-noise X-band oscillators. At the same time, the miniaturization and integration of precision photonic components through lithographic microelectronic fabrication have established a new paradigm in optical microsystem capability, cost, performance, and manufacturability. DARPA's GRYPHON program is leveraging emerging innovations in integrated photonics, nonlinear optics, and optical frequency division to develop microwave sources that are simultaneously compact, low noise, widely tunable, robust, and volume-manufacturable to enable disruptive sensing and communication capabilities.

4.2: **An Ultra-low Phase Noise Photonic Microwave Synthesizer** **(1:50)**

Jiang Li
hQphotonics Inc, Pasadena, CA

Mian Zhang, Prashanta Kharel
HyperLight Corporation, Cambridge, MA

4.3: **HIPPOGRIFFS: Hybrid-Integrated Packaged Photonic Oscillator Generating RF Using Internal Fast Frequency Synthesis** **(2:10)**

Mackenzie Van Camp
BAE Systems FAST Labs, Merrimack, NH

To meet current and future mission requirements, the DoD requires "rack-mount" reference oscillator phase noise performance in a compact, low-power package. BAE Systems is developing the HIPPOGRIFFS module on the DARPA GRYPHON program, providing low phase noise, sub-ns agility, and <100 Hz fine frequency steps across a 1 40 GHz output range in a 10cc, 10W package. We combine an ultra-stable 50 GHz photonic reference clock source with a chip-scale DDS circuit to tune across the full bandwidth, combining the precision of photonics with the agility of electronics. We shrink precision laser control electronics to a single integrated circuit and integrate the photonic subsystem on an ultra-low-loss silicon nitride platform, addressing the main limiting factors driving photonic oscillator system size. We use photonic wirebonds to bridge between optical elements, eliminating the need for active alignment. HIPPOGRIFFS drastically improves size, weight, power, and cost, expanding transition opportunities to UAVs and smaller systems.

4.4: Generating Optical Frequency Combs through Intracavity Phase Compensation **(2:30)**

Matthew W. Puckett, Chad W. Hoyt, Jianfeng Wu, Karl D. Nelson
Honeywell Aerospace, Honeywell, Charlotte, NC

Curtis R. Menyuk, Logan Courtright
University of Maryland, Baltimore County, Baltimore, MD

Jonathan Hu, Joshua T. Young
Baylor University, Waco, TX

Steven T. Cundiff, Grace C. Kerber
University of Michigan, Ann Arbor, MI

We describe a new technique for generating optical frequency combs (OFCs) from linear, silicon nitride (SiN) micro-resonators. Rather than relying on relatively thick SiN comb designs to yield intrinsic anomalous dispersion, here we engineered dispersion using intracavity Bragg gratings of various designs. We generated combs in 160 nm-thick linear resonators with chirped-period reflection gratings, resulting in comb spectral widths of approximately 2.5 nm and a resonator free spectral range of approximately 5 GHz. The spectral width can be increased by further engineering the cavity dispersion. Waveguide loss was 1 dB/m at 1585 nm and threshold pump powers were as low as 50 mW. These results open a path for OFCs to be generated in any waveguide platform with sufficiently low loss, making this technology more widely accessible and broadly applicable.

4.5: Compact, Heterogeneously-integrated, High-performance Microwave Signal Source **(2:50)**

Kerry Vahala, Andrey Matsko
California Institute of Technology, Pasadena, CA

Peter Rakich
Yale University, New Haven, CT

Steven Bowers, Joe Campbell
University of Virginia, Charlottesville, VA

Frank Quinlan
National Institute of Standards and Technology, Boulder, CO

Scott Diddams
University of Colorado, Boulder, CO

John Bowers
University of California, Santa Barbara, Santa Barbara, CA

We describe progress towards a heterogeneously-integrated, high-performance microwave-signal-source based upon optical frequency division. In the chip-based system, a microcomb is combined with two, ultra-narrow linewidth semiconductor lasers to transfer frequency stability from a compact optical reference cavity into an electrical microwave signal. The performance of all sub-systems will be reviewed and the status of the overall system performance will be provided.

BREAK supported by CADENCE **(3:10–3:30)**
Golden State Ballroom

Session 5

ADVANCES IN MULTI-CHIP INTEGRATION

Tuesday, 21 March / 1:30 – 3:10 pm / Palms Room 1-3

Chair: **Daniel Radack**
Institute for Defense Analysis, Alexandria, VA

Co-Chair: **Vashisht Sharma**
Institute For Defense Analyses, Alexandria, VA

5.1: **RESHAPE (Reshore Ecosystem for Secure Heterogeneously Advanced Packaged Electronics)** **(1:30)**

Donna Joyce, Peter O'Donnell
Army DEVCOM AvMC, Protective Technologies Division, Redstone Arsenal, AL

5.2: **The New Era of Innovation in 3DHI Microsystems: Tools, Flows, and Methodologies** **(1:50)**

Kenneth Larsen
Synopsys, Inc., Mountain View

The adoption of 3D Heterogeneous Integration and advanced packaging technologies is limited in the tools and expertise required to take advantage of the manufacturing possibilities. 3DIC design collapses traditionally separate disciplines – IP, chip, and package design – into a single design team. 3DIC requires new systems methodologies that span heterogeneous design, materials, multi-physics analysis, physical implementation, and verification. 3DHI also introduces new requirements for co-design and analysis to newly integrated design teams unfamiliar with them. This paper presents recent advances and directions in tools. flows and methodologies for the new era of innovation in 3DHI microsystems.

5.3: **Transitioning from 3D Packaging to 3D Heterogeneous Integration (3DHI)** **(2:10)**

John Park
Cadence Design Systems, San Jose, CA

Semiconductor packaging engineers have been heterogeneously integrating chips and designing 3D packages for over a decade. They used terms like multi-chip module (MCM), and system in a package (SiP) to describe these architectures. Over the past few years, a new vernacular has emerged based on a new set of acronyms – 3DHI, 3D-IC, and chiplets. In a large part, this new vernacular comes from semiconductor foundries and IC designers as they pivot from Moore's Law to the world of More-Than-Moore (3DHI). The two worlds of system design and IC design are beginning to merge, impacting design teams who are now required to define new design methodologies across a much wider set of EDA tools. This presentation outlines the nuances between 3D packaging and silicon stacking from a design methodology perspective and outlines many of the challenges designers can expect to face as they pivot to the world of More-Than-Moore.

5.4: Advanced SiP Packaging – Design, Assembly and Quality Considerations for Heterogeneous Integration **(2:30)**

Matt Bergeron, Sultan Lilani
Integra Technologies, Milpitas, CA

In today's advanced packaging world; we hear a lot about heterogeneous integration. The concept of heterogeneous integration evolves from the next level of advancement of system-in-package concept. The need for heterogeneous integration comes from system integrator's desire to simplify the system board design, increase I/O counts and increase functionality per unit area, with reduced board size. They are targeting to provide more system performance in less space with better electrical performance, reduced parasitics and reduced manufacturing costs. The integration of various functionalities requires older and newer microcircuit technologies to be within the same heterogeneous integrated package. This has posed some challenges from design, testability, yield, and qualification perspective. This paper will address the key engineering considerations from over-all design of the package along with substrate floor plans and assembly design rules. This paper will also discuss layout and fabrication of substrate along with over-all package testability, yield, and qualification challenges.

5.5: Glass-Core High Density Build Up (HDBU) Interposer for Future Advanced Packaging **(2:50)**

Kaysar Rahim, David Shahin, Brian Heldmann
Northrop Grumman Mission Systems, Baltimore, MD

Lakshminarasimha Vijaykumar, Xiaofan Jia, Mutee ur Rehman, Kai-Qi Huang, Chris, Fuhan Liu, Mohanalingam Kathaperumal, Jack Moon, Madhavan Swaminathan
Georgia Institute of Technology, Atlanta, GA

BREAK supported by CADENCE **(3:10–3:30)**
Golden State Ballroom

Session 6

ADVANCED GaN TECHNOLOGIES & APPLICATIONS

Tuesday, 21 March / 3:30 – 5:10 pm /
Town and Country Ballroom A

Chair: **Paul Maki**
Office of Naval Research, Arlington, VA

Co-Chair: **Gregg Jessen**
MACOM, Lowell, MA

6.1: **Fully Passivated AlN/GaN based T3.5 HEMT Device with 56% PAE and 1.2 db NFmin at 94 GHz** **(3:30)**

Erdem Arkun, Daniel Denninghoff, Andrea Corrion, David Fanning, Haidang Tran
HRL Laboratories, Malibu, CA

Future radars, electronic warfare and communication systems for the DoD applications require highly efficient, high power amplifiers (PA), low noise amplifiers (LNA) to be operating at mm-wave frequencies and beyond. HRL's T3 RF-GaN technology node is currently available to DoD and commercial customers through multiple technology access points including an MPW open foundry model. HRL is also investing in future nodes of fabrication technologies to concurrently offer scaled devices and circuits using the same access vehicles. In this paper we present our device results on T3.5 RF-GaN technology which was developed in the DARPA MGM program.

This research was developed with funding from Defense Advanced Research Projects Agency (DARPA). Any opinions, findings and conclusions, or recommendations expressed in this material are those of the author(s) and do not necessarily reflect the views of the United States Air Force.

6.2: **SSWEEt-STAr: Filling the Terahertz (0.1–20 THz) Solid State Amplifier Gap** **(3:50)**

Solomon Mikael, Benjamin Grisafe, Shawn Keebaugh, Shamima Afroz, Timothy Vasen, Robert Howell
Northrop Grumman Mission Systems – ATL, Linthicum, MD

John Volakis, Dimitris Pavlidis, Michail Anastasiadis, Abe Akhiyat, Nezih Pala, Shubhendu Bhardwaj
Florida International University, Miami, FL

6.3: **Recent Advances in S-band High Power Amplifiers with a 2 kW GaN Transistor Operating at 100 V** **(4:10)**

Gabriele Formicone, Apet Barsegyan, Jeffrey Burger, Richard Keshishian, Mahesh Kumar
Integra Technologies, Inc., El Segundo, CA

A single GaN transistor power amplifier with 2kW peak power level for S-band Air Traffic Control radar systems is presented. The uniqueness of this solid-state power amplifier is based on the novel RF AlGaN/GaN on SiC transistors which can be operated at 100 V bias rather than standard 50 V. The amplifier covers the frequency range of 2.7–2.9 GHz with a signal of 100 us pulse width and 10% duty cycle. The paper discusses recent advances implemented over a 1.5 kW GaN transistor amplifier for the same application that has recently been published at the 2022 European Microwave Integrated Circuit Conference.

6.4: Broadband Watt-Level Millimeter-Wave PA Design in 40-nm GaN HEMTs **(4:30)**

Clint Sweeney, Jill Mayeda, Donald Y.C. Lie
Texas Tech University, Lubbock, TX

Jerry Lopez
NoiseFigure Research Inc.
and
Texas Tech University, Lubbock, TX

We present several design examples with measurement data to suggest the barriers and paths to realize Watt-level broadband millimeter-wave (mm-Wave) power amplifiers (PA) using a low-voltage state-of-the-art 40-nm gallium nitride (GaN) high-electron-mobility transistor (HEMT) process. Very good agreement on measured vs. electromagnetic (EM) simulated results were observed, however, device breakdown can become an issue as discovered in measurement. Initially, at 21/24/28/31 GHz, the CS/2-stacked PA attained measured saturated output power ($P_{OUT,SAT}$) of 23.2/24.6/23.2/ 23.3 dBm with large signal gain above 20 dB. As the PA was measured under hotter biasing conditions where the DC bias voltage V_{DS} across each device exceeded 12 V, PA degradation was observed in measurement under repeated tests. We conclude with an example showing that at least from EM simulations, one can still achieve broadband (BW ~ 100%) mm-Wave Watt-level PAs with these devices arranged in a stacked PA topology to mitigate the breakdown/reliability issues.

6.5: GaN MMIC 4-Level Supply Modulator for PA Efficiency Enhancement **(4:50)**

Paul Flaten, Connor Nogales, Zoya Popović
University of Colorado, Boulder, CO

Joshua Hawke
U.S. Naval Surface Warfare Center, Crane, Crane, IN

EXHIBITOR RECEPTION **(6:00–8:00)**
Golden State Ballroom

Session 7

QUANTUM NETWORKS

Tuesday, 21 March / 3:30 – 5:10 pm /
Town and Country Ballroom B

Chair: **Michael Lovellette**
The Aerospace Corporation, Chantilly, VA

Co-Chair: **Manuel Trejo**
DoD

7.1: **Experimental Ambitions for DC-Area Quantum Network Testbed** **(3:30)**

Oliver Slattery
National Institute of Standards and Technology, Gaithersburg, MD

Adam T. Black
U.S. Naval Research Laboratory, Washington, DC

7.2: **Towards the Quantum Internet: Building an Entanglement-sharing Quantum Network in New York** **(3:50)**

Eden Figueroa
Stony Brook University / Brookhaven National Laboratory, Stony Brook, NY

Faithfully transferring quantum states between distant sites is the ultimate goal of quantum communication. The key aspect to achieve this is the generation of entangled states over long distances. However, the entanglement rates generated between two distant sites decrease exponentially with the length of the connecting channel. To overcome this difficulty, the new concepts of entanglement swapping, and quantum repeater operation are needed. We will show our progress towards building a quantum network of many quantum devices capable of distributing entanglement over long distances connecting Stony Brook University and the Brookhaven National Laboratory on Long Island, New York. We will show how to produce photonic quantum entanglement in the laboratory and how to store it and distribute it by optically manipulating the properties of atomic clouds. Finally, we will discuss our recent experiments in which several quantum devices are already interconnected forming an elementary version of a quantum-enabled internet.

7.3: **Quantum Optical Management for the DC-QNet** **(4:10)**

Abdella Battou
NIST, Gaithersburg, MD

A quantum optical network for DC-QNet will be described.

7.4: **Simulation Tools for Understanding Realistic Quantum Network Performance in Metropolitan and Tactical Environments** **(4:30)**

Brian Kirby, Dashiell Vitullo, Daniel Jones, Trevor Cook, Lisa Scott, Andrew Toth
DEVCOM Army Research Laboratory, Adelphi, MD

In this presentation we provide an overview of quantum network simulation tools in development at ARL. We then discuss how the Army aims to leverage these tools for better understanding the potential impact of quantum networks on tactical operations. Finally, we describe future plans to simulate the proposed DC-QNET metropolitan network.

7.5: New York Quantum Network: From Local to Regional **(4:50)**

Gabriella Carini
Brookhaven National Laboratory, Upton, NY

The BNL/SBU team has built one of the longest and most advanced quantum networks with 98 miles already operational (since 2020) and a recent expansion to 161 miles and five nodes covering Long Island from the two campuses to New York City. Additionally, some of this infrastructure has become available to the community as the first quantum network facility open to outside users. A first instance of hybrid quantum/classical network has been demonstrated as well as the first version of a Quantum Network Control Protocol (QNCP) to remotely control quantum and classical devices and subsystems of the BNL/SBU quantum internet testbed. Several other successful experiments have created the basis to expand further this effort and build a larger initiative in New York State with several key partners looking into novel applications of entanglement distribution network. Details of the current status and plan will be presented.

EXHIBITOR RECEPTION **(6:00–8:00)**
Golden State Ballroom

Session 8

TRUST VERIFICATION AND VALIDATION

Tuesday, 21 March / 3:30 – 5:10 pm /
Town and Country Ballroom C

Chair: **Saverio Fazzari**
Booz Allen Hamilton, Clarksville, MD

8.1: **Turn-Key Compressed Sensing System for Electron Microscopy** **(3:30)**

E. L. Principe
Synchrotron Research, Inc., Melbourne Beach, FL

J. J. Hagen, B. W. Kempshall, K. M. Scammon
PanoScientific LLC, Cocoa, FL

8.2: **Physically-aware Laser Fault Injection Assessment** **(3:50)**

Henian Li, Sukanta Dey, Farimah Farahmandi
University of Florida, Gainesville, FL

Laser-based fault injection (LFI) attacks are powerful physical attacks with high precision and controllability. Several works in literature attempt to model and simulate the laser effect in pre-silicon digital designs, including RTL, SPICE and TCAD models. However, these fault models are neither scalable nor account for actual laser fault simulation. In this paper, for the first time, we propose a physical layout-level LFI assessment framework to verify the layout's resiliency against LFI. The proposed framework can inject Gaussian laser current profiles of any spot size into the physical layout. To make it scalable, we perform SPICE simulations, and employ machine learning to develop cell-level laser fault models which can capture the current characteristics of every standard cell, under different laser-induced transient current intensities. This laser cell library is then utilized during laser fault simulation. Finally, we demonstrate effectiveness of the proposed framework by analyzing the fully implemented AES design layout.

8.3: **A Comparative Analysis of Broad and Focused Ion Beam Techniques for Backside Material Removal of a 14 nm Node FinFET Device** **(4:10)**

Yash Patel, Jonathan Scholl, Adam R. Waite, John Kelley, Adam Kimura
Battelle Memorial Institute, Columbus, OH

Richard Ott, Glen David Via
Air Force Research Laboratory, Wright-Patterson AFB, OH

8.4: Automated Formal Equivalency Checking for FPGA Tools **(4:30)**

Christopher R. Clark, William Stuckey, Nathan Braswell
Georgia Institute of Technology, Atlanta, GA

Travis Haroldsen, Ting-Yuan Sung, Osaze Shears
University of Southern California, Arlington, VA

EDA tools that perform synthesis, placement, and routing are necessary to translate HDL source code to an FPGA implementation netlist. However, this process can introduce undesired functional changes to the design, which may be the result of bugs in optimization algorithms or malicious modifications to the software. Formal equivalency checking (FEC) is an effective approach to address these concerns, but the difficulty and high level of effort required to apply this technique are impediments to widespread adoption. In this paper, we present a software framework that automates the configuration and execution of FEC tools. Automated analysis of logs and netlists produced by EDA tools is used to identify design optimizations and generate corresponding compare point mapping directives, or hints, that are required for effective and efficient formal analysis. The developed framework supports multiple commercial and open-source EDA and verification tools and easily integrates with existing implementation flows.

8.5: Back End of Line GDS-II Verification Through X-ray Tomography **(4:50)**

Michael Sutherland
Defense Microelectronics Activity, McClellan Park, CA

EXHIBITOR RECEPTION **(6:00–8:00)**
Golden State Ballroom

Session 9

ADVANCED PACKAGING AND INTEGRATION

Tuesday, 21 March / 3:30 – 5:10 pm /
Town and Country Ballroom D

Chair: **Wes Hansford**
Boeing, Huntington Beach, CA

Co-Chair: **T. Robert Harris**
Georgia Tech Research Institute, Atlanta, GA

9.1: Solder-less Fine Pitch Copper to Copper Bonding (3:30)

Nicholas Lay, Kaysar Rahim
Northrop Grumman, Baltimore, MD

In this study, we have reported the development of a direct copper to copper bonding innovation. Our process differs from common hybrid bonding copper to copper techniques, it is designed for low volume highly complex products. The technology allows a die-to-die direct copper bonding processes ideal for high power, high thermal applications. The process does not require high temperature oven annealing and can be done in normal atmospheric environment. Process developed employs a thermo-compression bonding method, utilizing a deoxidizing gas to allow for direct copper to copper bonding to occur. This process offers a low cost, reliable method for vertically stacking of higher-cost devices.

9.2: Selective Cobalt Atomic Layer Deposition for Chiplet Heterogenous Integration Technology (3:50)

Madison Manley, Ming-Jui Li, Muhannad Bakir
Georgia Institute of Technology, Atlanta, GA

Zachary Deveraux, Nyi Myat Khine Linn, Charles Winter
Wayne State University, Detroit, MI

Andrew Kummel
University of California San Diego, San Diego, CA

There is a growing interest in 3D heterogenous integration technologies due to their dense interconnections between chips and low latency and power consumption. In this work, we will demonstrate a 3D integration technology that enables ultra-dense I/O bonding to approach on-chip via densities using cobalt selective atomic layer deposition (Co ALD). The goal is to demonstrate an array of chiplets simultaneously 'bonded' to a wafer using selective deposition of the I/O interconnect bonds onto the aligned copper pads. Test beds containing Cu/Gap/Cu lateral and vertical test structures will be demonstrated with the gap sizes range from 50 nm–200 nm and pitches range is 1 µm–10 µm. The results show the feasibility of using selective Co ALD as high-density Cu-Cu interconnect bonding. SEM and XPS are used to characterize the testbed before and after Co deposition and to measure the selectivity of Co ALD on the Cu and Si_3N_4 substrate.

9.3: Bimorph Cantilevers as Flexible RF Interconnects to Enable Heterogeneous Integrated Microsystems **(4:10)**

David Torres Reyes, William Gouty, John L. Ebel
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

Gerardo L. Morales, Juan J. Pastrana
Michigan State University, East Lansing, MI

9.4: RF Heterogeneous Integration using Photosensitive Glass Ceramics **(4:30)**

Jeb Flemming, Kyle McWethy, Rohan Netto
3D Glass Solutions, Albuquerque, NM

3DGS presents a manufacturing platform for the production of vertically stacked glass substrates with integrated high Quality Factor passive devices, such as inductors and capacitors, and heterogeneously integrated surface mount devices for advanced RF systems-in-package. The presented material demonstrates a production and assembly process for the manufacturing of advanced systems. In this paper, we present design, production, assembly considerations that impact size, weight, and performance (SWAP) metrics for a variety of product definitions and multiple simulation vs. product testing to demonstrate a reliable design to product flow.

9.5: Applications of Additive Manufacturing in the Microelectronics Advanced Packaging Landscape **(4:50)**

Ashley Batjer, Ryan Eames, Rory Burke, Brandon Hamilton, Chris Riso, Julian Warchall, Saverio Fazzari
Booz Allen Hamilton, McLean, VA

Darren Crum
U.S. Department of the Navy, Crane, IN

EXHIBITOR RECEPTION **(6:00–8:00)**
Golden State Ballroom

Session 10

DSSoC

Tuesday, 21 March / 3:30 – 4:50 pm / Palms Room 1-3

Chair: **Thomas Kazior**
Raytheon Technologies, Goleta, CA

Co-Chair: **Johnny Marsh**
DARPA, Arlington, VA

10.1: Test and Evaluation for the DARPA DSSoC Program: Evaluating Software for Open Source Hardware Community Impact **(3:30)**

Annika Horgan, John Wohlbier
Carnegie Mellon University, Pittsburgh, PA

The DARPA Domain-Specific System-on-Chip (DSSoC) program aims to ease programmability of heterogeneous chips, where the deliverables are both physical system-on-chip (SoCs) specialized for specific domains and software stacks to deploy applications and design next generation chips. The DSSoC program emphasizes programmability because long-term success for DSSoC chips requires quick turn-around development times for integrating hardware or application improvements. The DSSoC Broad Agency Announcement (BAA) encourages performers to open-source software where wide community exposure will maximize the program's impact on growing industry adoption of heterogeneous hardware. Test and Evaluation (T&E) focused on usability and robustness for software users and developers while also verifying reported capabilities. Because usable and robust tools are important both for DoD transition and long-term impact beyond DoD, a flexible T&E focused on identifying risks and giving feedback to performers will help maximize long-term program impact while other parties are focused on pushing innovation on tight deadlines.

10.2: Integrating 5G Stand Alone on the DASH v1.0 Processor **(3:50)**

Lucas Zmroczek, Peter Koop, Clayton Uhing, Joshua Brunk, Daniel Connolly
Johns Hopkins University – Applied Physics Laboratory, Laurel, MD

10.3: Software-Hardware Co-Design of Domain-Specific SoCs: The EPOCHS Experience Report **(4:10)**

Pradip Bose, Augusto Vega
IBM T. J. Watson Research Center, Yorktown Heights, NY

Luca Carloni, Ken Shepard
Columbia University, New York, NY

David Brooks, Vijay Janapa Reddi, Gu-Yeon Wei
Harvard University, Cambridge, MA

Sarita Adve, Vikram Adve, Sasa Misailovic
University of Illinois at Urbana-Champaign (UIUC), Urbana, IL

Intelligent edge systems constitute a key growth segment within the cloud-backed cognitive IoT marketplace. The EPOCHS research project is driven by the specific edge application domain of connected autonomous vehicles. Our team has developed leading edge methodologies for agile software-hardware co-design of heterogeneous SoCs to support the target application domain. As part of this project, we have successfully taped out two EPOCHS chips in 12 nm technology, and have demonstrated full-stack solutions using FPGA versions of the chipset. Specific use cases illustrated are: (a) collaborative perception, involving a pair of communicating autonomous vehicles; (b) detecting hazards while scanning for objects and vehicles during autonomous navigation; (c) sentiment analysis of human-expressed conversations or commands (using an NLP algorithm) in a setting where a passenger (or passive driver) interacts with an autonomous navigation system. We discuss specific technology transition opportunities in this (the final) phase of DARPA's DSSoC program.

10.4: Implementation Examples on a Course-Scale Heterogeneous Processor **(4:30)**

D. W. Bliss, J. Brunhaver, S. Bryan, C. Chakrabarti, L. Chang, X. Chen, A. R. Chiriyath, A. Dutta, Y. Fu, A. Herschfelt, J. Holtom, Y. Li, Y. Liu, R. LiKamWa, O. Ma, B. McCall, S. Siddiqui, D. Silbernagel, A. Venkataramani, B. R. Willis, H. Yu
Arizona State University, Tempe, AZ

T. Ajayi
Arizona State University, Tempe, AZ
and
University of Michigan, Ann Arbor, MI

A. Akoglu, S. Gener, Md. S. Hassan, J. Mack
University of Arizona, Tucson, AZ

D. Blaauw, L. Belayneh, K.-Y. Chen, M.-H Chen, R. Dreslinski, H.-S. Kim, T. Mudge, X. Wei, Y. Yue
University of Michigan, Ann Arbor, MI

A. Goksoy, A. N. Krishnakumar, S. K. Mandal, U. Y. Ogras, V. Pandey
University of Wisconsin–Madison, Madison, WI

R. Marculescu
University of Texas at Austin, Austin, TX

EXHIBITOR RECEPTION **(6:00–8:00)**
Golden State Ballroom

WEDNESDAY, 22 MARCH

Continental Breakfast **(7:30–8:30)**

Session 11

STARRY NITE

Wednesday, 22 March / 8:20 – 9:40 am /
Town and Country Ballroom A

11.1: RF & Optoelectronics Technical Execution Area Project "STARRY NITE": State-of-the-Art Radio Frequency Gallium Nitride Foundries **(8:20)**

Joshua Hawk, Brian Olson, Vincent Williamson
U.S. Naval Surface Warfare Center, Crane, IN

Eric Kamp
Booz Allen Hamilton, McLean, VA

Gallium Nitride on Silicon Carbide is the only semiconductor in production that allows access to mmW frequencies with minimized size, -weight, and -power (SWAP). U.S. leadership in this critical technology has been threatened in the last several years as international demand for RF GaN technologies has driven foreign countries to expand their manufacturing bases. The State-of-the-Art Radio Frequency Gallium Nitride Foundry (STARRY NITE) project plans to address this by maturing mmW nodes, advanced interconnect processes, and providing multi-project wafer runs to demonstrate these services. Utilizing the Manufacturing Readiness Level (MRL) Deskbook and applying it to the foundry nodes and advanced interconnect processes at three demonstrator sites, STARRY NITE will scale mmW foundry maturity towards production. This will be demonstrated through multiple MPW runs per year which will evaluate these capabilities and provide access to mmW device designers within the DoD.

11.2: Manufacturing Improvements in 40-nm T3 GaN HEMT MMIC Process **(8:40)**

David Fanning, Andrea Corrion, Georges Siddiqi, Dan Denninghoff, Erdem Arkun, Harris Moyer, Ignacio Ramos, Andy Fu, Dave Chow, Martin Galan, Shyam Bharadwaj
HRL Laboratories, Malibu, CA

Nicholas Miller, Michael Elliott
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

HRL's T3 GaN MMIC process is a versatile process suitable for operation up to 160 GHz for transmit and receive applications required by defense and commercial customers. T3 GaN features a highly scaled AlN/GaN HEMT epitaxial stack, regrown ohmic contacts, and a 40-nm gate length. While these are excellent for performance, they also present manufacturing challenges. Under internal and government funding, we have matured T3 GaN and have begun offering it as a foundry service. We have improved the manufacturability aspects of yield, uniformity, and cycle time. The process is at Manufacturing Readiness Level (MRL) 5 and we anticipate MRL 8 by January of 2025 under the Starry Nite program. Both measured and modeled discrete device and MMIC performance from Ka- to W-band will be presented, including results from a newly updated Angelov-based compact circuit model.

11.3: Maturation of Northrop Grumman's 90 nm GaN Technology for W-band Applications **(9:00)**

Robert Coffie, Jansen Uyeda, Emily Pollock, Sumiko Poust, Hui Ma, Xiang Zeng, Ben Poust, Mike Barsky, Farman Mesdaghi, Wesley Chan, Randy Sandhu, David Shahin, Lesley Cheema, Megan Ratajczak, Ke Luo, James Patten, Sahand Noorizadeh, Ben Heying, Aaron Oki
Northrop Grumman Corporation, Redondo Beach, CA

11.4: Maturing 90 nm GaN with Advanced Interconnect Technology on 150 mm Substrate for Millimeter Wave Systems **(9:20)**

Vipan Kumar, Deep Dumka, Chuanxin Lian, Ray Li, Andy Xie, Gergana Drandova, John Hitt, Jose Jimenez, Antonio Lucero, Shuoqi Chen, Scott Schafer, Anthony Chiu, Tarak Railkar, Vivian Li, Paul Schmid, Cathy Lee
Qorvo, High Performance Analog, Systems and Research, Richardson, TX

BREAK Supported by Microsoft Corp. **(10:00–10:30)**
Golden State Ballroom

Session 12

DREaM

Wednesday, 22 March / 8:20 – 10:00 am /
Town and Country Ballroom B

Chair: **Thomas Kazior**
Raytheon Technologies, Goleta, CA

Co-Chair: **Gregory Jones**

12.1: Millimeter-wave ScAlN/GaN-based Heterostructure Field Effect Transistors and MMICs (8:20)

Eduardo M. Chumbes, John Logan, Brian Schultz, Matt DeJarld, Maher Tahhan, Yan Chen, Nick Kolias
Raytheon Company, Andover, MA

Matt Hardy, Mario Ancona, Neeraj Nepal, David Meyer
U.S. Naval Research Laboratory, Washington, DC

At GOMAC 2022, we reported our latest generation of W-band transistors based on ScAlN/GaN heterostructure delivering >5 W/mm with >10% PAE at 94 GHz. Those transistors were utilized to demonstrate for the first time a wideband (20–40 GHz) MMIC achieving >3 Watts with >10% PAE across the band. We will present results on our next generation ScAlN/GaN transistors and MMICs incorporating several epi and process enhancements aimed at maximizing gain while reducing DC/RF dispersion and off-state leakage necessary to exceed the DARPA Dynamic Range-enhanced Electronics and Materials (DREaM) Phase 2 metric goals of 10 W/mm with 1 W total power and 35% PAE at 94 GHz.

This work is supported in part under the DARPA DREaM Program under the direction of Drs. T. E. Kazior and Y K Chen (contract no. FA8650-18-C-7806 monitored by David Via and Nicholas Miller – AFRL).

12.2: Demonstration of SLCFET Amplifier Technology with 10.8 W/mm and 43.2% PAE at 94 GHz (8:40)

Brian Novak, Timothy Vasen, Patrick Shea, Robert S. Howell, Josephine Chang, Shamima Afroz
Northrop Grumman Mission Systems, Linthicum, MD

12.3: Highly-linear and Efficient Ka-band and W-band MMIC Amplifiers (9:00)

Jeong Moon, Bob Grabar, Joel Wong, Chuong Dao, Erdem Arkun, Hwa Tai, Ignacio Ramos, Shyam Bharadwaj, Dave Fanning
HRL Laboratories, Malibu, CA

High dynamic range RF front-ends in phased array systems are increasingly important due to the increased jamming or interference, where the RF system jamming margin can be improved by 6.7× when the RF system linearity increases by 10×. Under the DARPA DREaM program, we demonstrated linear graded-channel GaN HEMTs with mini-field-plate gate, and demonstrated excellent fT and fMAX of 200 GHz and 350 GHz, respectively. With the graded-channel GaN HEMTs, we demonstrated low-noise and linear 20–40 GHz GaN MMICs with a 1.3–2 dB noise figure and with a state-of-the-art output third-order intercept point (OIP3) of 36 dBm at 30 GHz, demonstrating the record linearity figure-of-merit, OIP3/PDC, of 17.5 dB. With a minimal current collapse, the graded-channel GaN HEMTs demonstrated SOA W-band performance with peak power-added efficiency (PAE) of 50% and 42% at 2.2 W/mm and 3.5 W/mm at 94 GHz at the device level, respectively. We will report on the performance of high-power W-band amplifiers.

12.4: Increased N-polar GaN W-band Power above 700 mW and Efficiency above 40% **(9:20)**

Matthew Guidry, Emre Akso, Weiyi Li, Henry Collins, Christopher Clymore, Robert Hamwey, Christian Wurm, Pawana Shrestha, Wenjian Liu, Brian Romanczyk, Nirupam Hatui, Stacia Keller, Umesh Mishra
University of California, Santa Barbara, CA

N-polar GaN deep recess MISHEMT devices have previously shown excellent mm-wave CW transmit power performance with 94 GHz power density up to 8.8 W/mm (660 mW) at an associated 27% PAE, and power density of 6.2 W/mm (465 mW) at 34% PAE. These prior demonstrations used cells with two gate fingers and 75 microns of total periphery. This work presents demonstrations in two key areas. First, scaling the total output power with larger cell peripheries to reach 712 mW at 32% PAE at 20 V bias, a record single-device output power at 94 GHz. And second, increasing the gain and efficiency with an improved gate process and lower parasitic capacitance so that 4.4 W/mm power density could be reached at 42% PAE, a record combined power density and efficiency.

12.5: Progress Towards a W-Band GaN-on-SiC HEMT in a Production Silicon Fab **(9:40)**

James G. Fiorenza, Daniel Piedra, Pete Stubler, Leslie Green, Guanghai Ding, Xiaowei Cai, Denis Murphy, Yingqi Jiang, Andrew Proudman, Elbert Chang, Jake Steigerwald, Susan Feindt
Analog Devices Inc., Wilmington, MA

This talk will describe recent progress towards the development of a W-Band GaN-on-SiC HEMT process using a production silicon fab and using silicon-like device design techniques. Compared to the traditional gold-based resist-liftoff approach for processing III-V materials, fabrication of microwave GaN devices in a silicon fab improves device yield and manufacturability by taking advantage of advanced tool sets, and well controlled deposition and etch process modules shared by Si processes. The adaptation of silicon-like device design techniques enables the exploitation of field control techniques that are widely successful in maximizing silicon RF power device performance, but that have not previously been used in GaN HEMTs. This talk will update the progress made as part of the DARPA DREaM program.

BREAK Supported by Microsoft Corp. **(10:00–10:30)**
Golden State Ballroom

Session 13

COUNTERFEIT DETECTION & AVOIDANCE

Wednesday, 22 March / 8:20 – 10:00 am /
Town and Country Ballroom C

Chair: **Joel Goodman**
Navy Research Laboratory, Washington, DC

13.1: Self-contained LDO Odometer to Detect Recycled Counterfeit AMS Chips (8:20)

Sourav Roy, Domenic Forte
University of Florida, Gainesville, FL

JinHong Chen
The Ohio State University, Columbus, OH

Counterfeit electronics is a growing threat with widespread impacts on many aspects of modern civilization including defense, communication, healthcare, manufacturing industry, agriculture and all other areas dependent on integrated circuits (ICs) or chips. Among all the counterfeit types more than eighty percent are recycled chips. These are the chips that are taken from discarded, obsolete electronics board and then sold as new. Therefore, they are aged and deteriorated with short remaining lifespan, prone to failure etc. Research has been conducted to identify recycled chips but those methods are not equally applicable to all kinds of chips. Specifically, hardware security primitives are primarily developed for digital circuits and not easily ported to analog and mixed signal (AMS) chips. Recently, an LDO-based odometer was proposed which requires external measurements through exposed pins which is both expensive and vulnerable. In this work, we propose a self-contained design that overcomes these issues.

13.2: Modeling and Evaluation of a Counterfeit Detection System Using SPICE (8:40)

Carl Bohman, Christian Eakins, Aaron Jennings, Ryan Lachey, Mark Skouson
KBR, Beavercreek, OH

Jamin McCue, Richard Ott
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

This work outlines the use of a SPICE simulator to evaluate the sensitivity and performance of a counterfeit detection system. Specifically, the simulator enables the detection system to interrogate parts with known deviations, parameter distributions, and architectural changes while providing an efficient way of increasing the population size to one of statistical relevance. For this work, a light-weight simulator (LTSPICE) is used to demonstrate the feasibility of this evaluation technique. Additionally, sensitivity analysis is possible, facilitating the determination of critical circuit parameters for counterfeit discrimination.

13.3: Exploration of Automated Laser Marking Analysis for Counterfeit IC Identification **(9:00)**

Jacob Harrison, Nathan Jessurun, Mark Tehranipoor, Navid Asadi
University of Florida, Gainesville, FL

Fraudulent and counterfeit microelectronics are a threat to the reliability of critical systems, but thorough counterfeit screening is costly. As a result, efficient, automated detection techniques are needed. This work explores the potential for granular characteristics of laser-etched part numbers, lot numbers, and logos to serve as a per-packaging-facility fingerprint and, therefore, as evidence of component provenance. Initial research suggests that etcher capabilities and configurations, such as first-pulse control, etch-over vs. skip-over stroking, mirror calibration, and others, can be inferred from a marked chip. While prior work has noted that low-quality markings are cause for suspicion, we are the first to correlate specific, automatically-extractable marking characteristics that result from laser etcher configuration. Our results could lead to real-time counterfeit detection that leverages existing hardware, such as cameras in pick-and-place machines.

13.4: Simulation and Analysis of a Process-of-Origin Identification Technique Using the Process Specific Functions of Bandgap Voltage References **(9:20)**

Daron DiSabato, Dale Shane Smith, Waleed Khalil
The Ohio State University, Columbus, OH

Aaron Jennings, Ryan Lachey, Kurt Sakamoto, Carl Bohman, Christian Eakins
KBR US, Beavercreek, OH

Lucas Duncan
Niobium Microsystems, Dayton, OH

Jamin McCue
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

13.5: Low Cost Anticounterfeit PUF **(9:40)**

Pallavi Ebenezer, Degang Chen, Randall Geiger
Iowa State University, Ames, IA

A subthreshold PUF-embedded anticounterfeit circuit is proposed to mitigate the financial incentives that drive the counterfeit community and to encourage the COTS manufacturers to use authentication for system identification in their parts. The proposed design uses the inherent variations of the threshold voltage mismatch in cross-coupled inverters pairs due to process variations to generate the unique fingerprint. The PUF-embedded shift register does not require additional die area, pins, read-out circuitries, or power overhead. The performance of the primary circuit is unaffected by the fingerprint circuit as it operates at only 50% of the nominal supply. The proposed strategy which can generate a large number of bits per unit PUF cell has been designed and validated in a 65 nm CMOS process using transient noise analysis and Monte Carlo simulations.

BREAK Supported by Microsoft Corp. **(10:00–10:30)**
Golden State Ballroom

Session 14

INTEGRATED PHOTONIC CIRCUIT NEEDS, PLATFORMS, AND SYSTEMS

Wednesday, 22 March / 8:20 – 9:40 am /
Town and Country Ballroom D

Chair: **Nick Usecheck**
AFRL, Wright Patterson AFB, OH

Co-Chair: **Preetpaul Devgan**

14.1: **Broadband Optical Beamforming with Coherent Analog True Time Delay** **(8:20)**

Chunyan L. Lin, Christopher K. Huynh, Shai B. Jester, David W. Brock, Dennis Bermeo, James R. Adleman
NIWC Pacific, San Diego, CA

14.2: **Silicon Photonic Optical Phased Arrays and Hybrid Lasers for Coherent LiDAR Applications** **(8:40)**

Christopher V. Poulton, Peter Russo, Matthew J. Byrd, Benjamin Moss, Oleg Shatrovoy, Murshed Khandaker, David Paquette, Jiajiu Zheng, Jonathan Guglielmon, Andrew Reardon, Samuel Burck, Michael R. Watts
Analog Photonics LLC, Boston, MA

Silicon photonic optical phased arrays provide chip-scale solid-state beam steering. Combined with hybrid lasers and coherent receivers, FMCW LiDAR can be realized. We present results from the DARPA MOABB program including 8,192 element arrays, widely tunable narrow linewidth lasers, and a single-unit coherent LiDAR system with real-time range and velocity detection.

14.3: **Photonic Integrated Circuits: Assessment of State-of-the-Art Manufacturing Industrial Base Capabilities and Needs (PICASSO'S MUSICIANS)** **(9:00)**

Andrew Stark, Christian Bottenfield, B. Michael Kanack, T. Robert Harris, Leif Sandstrom, Brian Wier, Hannah Foster, Benjamin B. Yang
Georgia Tech Research Institute, Atlanta, GA

Todd Stievater, Peter G. Goetz, Joseph Singley
U.S. Naval Research Laboratory, Washington, DC

Joshua Hawke
NSWC Crane, Crane, IN

The PICASSO'S MUSICIANS study was executed to take a technological snapshot of silicon photonics in the US and is written for the purpose of providing recommendations for Department of Defense (DoD) stakeholders. The study aims to provide a broad overview of the silicon photonics landscape with a focus on DoD-specific application areas. This overview will allow DoD decision-makers to more successfully navigate the industry landscape for ensured technology access and maturation and to fill critical capability gaps. Recommended actions address two key categories of investments: (1) technology and (2) ecosystem and infrastructure. Silicon photonics technology is developing rapidly, largely fueled by commercial sector interest in data communications and telecommunications. However, key areas important to DoD priorities remain underinvested and underdeveloped.

14.4: Integrated Microwave Photonics **(9:20)**

Siva Yegnanarayanan, Dave Kharas, Jason J. Plant, Matt Ricci, Cheryl Sorace-Agaskar, Paul W. Juodawlkis
MIT Lincoln Laboratory, Lexington, MA

We review the latest advances in on-chip microwave photonics and describe recent demonstrations using Lincoln Laboratory's photonic multi-chip module (P-MCM) hybrid integration platform including high-power lasers, wideband modulators, reconfigurable optical filters and wideband high-saturation photodiodes, suitable for the realization of high-performance microwave photonic subsystems-on-a-chip.

BREAK Supported by Microsoft Corp. **(10:00–10:30)**
Golden State Ballroom

Session 15

STATE-OF-THE-ART HETEROGENEOUS INTEGRATION PACKAGING

Wednesday, 22 March / 8:20 – 9:40 am / Palms Room 1-3

Chair: **Darren Crum**
NSWC Crane Division, Crane, IN

15.1: **On Shore Advanced Microelectronics Packaging Usage & Capabilities** **(8:20)**

Brandon Hamilton, Chris Riso, Julian Warchall, Christopner Gregory, Joe Coye, Saverio Fazzari, Doug Palmer
Booz Allen Hamilton, Mclean, VA

Phil Garrou
Microelectronics Consultants of NC, RTP, NC

Darren Crum
U.S. Department of the Navy, Crane, IN

15.2: **A Study of the Global Capabilities in Advanced Packaging** **(8:40)**

Roshan Daniel, Chris Riso, Julian Warchall, Rory Burke, Ashley Batjer, Saverio Fazzari, Doug Palmer
Booz Allen Hamilton, Mclean, VA

Darren Crum
U.S. Department of the Navy, Crane, IN

15.3: **Glass Substrate-Based 3D RF System-in-Package** **(9:00)**

David Shahin, Andrew Cogliano, Michael Langlois, Girish Upadhya, Maxim Serebreni, Michael Spratley, Aaron Wescott, Sarah Woodworth, Courtney Wosepka, Matthew Doerflein
Northrop Grumman Mission Systems, Baltimore, MD

15.4: **Technology Characterization Vehicle Designs Using Glass-core Based Substrates for Millimeter Wave Applications** **(9:20)**

Shuoqi Chen, Yanghun Yun, Anthony Chiu, Rajanish Pandey, Andrew Ketterson, Kirk Ashby
Qorvo, HPA Systems and Research, Richardson, TX

This paper describes a set of technology characterization vehicle (TCV) designs and performances using the selected multi-layer glass-core based substrates for millimeter wave application in SHIP-RF phase I program. In this work microstrip, CPWG, strip line, and inverse microstrip transitions, as well as microstrip coupling structures have been designed and analyzed. Those TCVs were used to measure the performance of glass-core based interconnects up to 50 GHz and perform model to hardware correlation to confirm acceptability of the first pass electrical properties and RF performance. Especially, through glass via (TGV) transition has been characterized with 0.54 dB insertion loss and 0.12 nH inductance up to 50 GHz. The outstanding simulation performance shows this multi-layer glass-core based integration technology is a promising solution for millimeter wave applications.

BREAK Supported by Microsoft Corp. **(10:00–10:30)**
Golden State Ballroom

Session 16

WARP I

Wednesday, 22 March / 10:30 am – 12:10 pm /
Town and Country Ballroom A

Chair: **David Abe**
DARPA / Microsystems Technology Office

Co-Chair: **Steven Gross**
DARPA, Arlington, VA

16.1: **Highly Compact Reconfigurable Microwave Filters on Glass Substrates** **(10:30)**

Eric E. Hoppenjans
Indiana Microelectronics, LLC, West Lafayette, IN

16.2: **Highly-Linear Chip-Scale 2–18 GHz Tunable Multi-Notch Filters and Tunable Acoustic-Bandpass Filters** **(10:50)**

Matthew Morton, Gerhard Sollner, Charles Wang, Clay Long, Adam Peczalski, Matthew Rebholz
Raytheon Technologies, Andover, MA

Damla Dimlioglu, Thomas Tapen, Alyosha Molnar, Alyssa Apsel
Cornell University, Ithaca, NY

Armagan Dascurcu, Hari Vemuri, Harish Krishnaswamy
Columbia University, New York, NY

16.3: **Zero Static Power Tunable Magnetostatic Wave Filters** **(11:10)**

Xingyu Du, Yixiao Ding, Tao Zhang, Alexander J. Geers, Jun Beom Pyo, Mohamad Hossein Idjadi, Firooz Aflatouni, Mark Allen, Roy H. Olsson III
University of Pennsylvania, Philadelphia, PA

This paper reports on the demonstration of a miniature, frequency tunable, high quality factor, filter technology that consumes zero static power. The filter combines magnetostatic surface wave resonators, which are frequency tunable via external magnetic field, with a magnetic bias circuit that produces a nonvolatile magnetic bias field that is programmable from 450 G to 2900 G via current pulses. The filter demonstrates passband center frequency tuning from 3.2 to 10.2 GHz while maintaining an in-band insertion loss of less than 5.5 dB. The filter has a high IIP3 for signals lying outside the filter passband greater than +50 dBm. The filter, including the magnetic bias circuit, occupies a volume of 0.3 cubic centimeters and consumes zero static power.

16.4: **A Ku-Band Compact Wide-Tuning Filter for Arrays** **(11:30)**

Eric C. Wagner, Dah-Weih Duan, Alex Chau, Eric Kaneshiro, Ken Sato, Aaron Oki, Augusto Gutierrez-Aitken
Northrop Grumman Space Systems, Redondo Beach, CA

16.5: Wide Band, Frequency Adaptive Filter with Embedded Threshold Detection **(11:50)**

Michael Meholensky
Collins Aerospace, Cedar Rapids, IA

Charles Campbell
Qorvo, Richardson, TX

Piotr Kulik
Metamagnetics, Inc., Marlborough, MA

This paper describes the design and integration of a wideband, 2–18 GHz, low insertion loss tunable filter. Multiple technologies, including an intrinsically switched multiplexer (ISM) and a magnetic Auto-tune Filter (AtF), are used to achieve the band coverage. Designed to operate with wide-band receivers, the device senses and adapts the filter using integrate couplers and inherent material properties. Packaging will use an additive manufacturing process.

LUNCH Supported by SkyWater Technology **(12:00–1:30)**
Golden State Ballroom

Session 17

COFFEE

Wednesday, 22 March / 10:30 am – 12:10 pm /
Town and Country Ballroom B

Chair: **Benjamin Griffin**

Co-Chair: **Rocco Bogoslovov**
DARPA, Arlington, VA

17.1: A Manufacturable AlScN Periodically Polarized Piezoelectric Film Bulk Acoustic Wave Resonator (AlScN P3F BAW) Operating in Overtone Mode at 10.7 GHz (10:30)

Ramakrishna Vetury, Abhay Kochhar, Jeff Leathersich, Craig Moe, Mary Winters, Jeffrey Shealy
Akoustis Technologies Inc., Huntersville, NC

Roy Olsson
University of Pennsylvania, Philadelphia, PA

We report a manufacturable, Periodically Polarized Piezoelectric Film (P3F) Bulk Acoustic Wave (BAW) resonator using Aluminum Scandium Nitride (AlScN) materials. P3F BAW technology benefits from a significantly larger film thickness than the traditional BAW thickness-frequency scaling approach, enabling a manufacturable high frequency resonator technology with high Q-factors. We report fabricated P3F BAW resonators demonstrating 2nd overtone operation at 10.7 GHz with a FoM, (Qp × kt2) of 27. These results suggest that AlScN P3F BAW using overtone mode operation can enable miniature, manufacturable, high-performance filters for X-band and higher frequencies.

17.2: ARABIKA: The First Step Towards Miniaturized Front End Filtering (10:50)

Matthew Torpey, Robert S. Howell
Northrop Grumman Mission Systems, Linthicum, MD

Azadeh Ansari
Georgia Institute of Technology, Atlanta, GA

Zetian Mi
University of Michigan, Ann Arbor, MI

The Acoustic Resonator Multi-Mode Based Densely Integrated S-Ku Filters for Advanced RF Systems (ARABIKA) creates a breakthrough in filter size and performance, providing the warfighter with an asymmetrical advantage in confronting emerging threats by enabling wideband digital sensors to operate in a congested electromagnetic spectrum (EMS) without sacrificing performance (saturation, desensitization, false alarms) through EMS interference management prior to receiver digitization.

17.3: Heterogeneously Integrated Miniaturized Magnetic Wave Filters (11:10)

Matthew A. Laurent, Nancy Lin, Carson Goettlicher, Elizabeth Kunkee, Dino Ferizovic
Northrop Grumman Corporation, Redondo Beach, CA

Alexander Sokolov, Piotr Kulik, Michael Geiler
Metamagnetics, Inc., Westborough, MA

17.4: Miniaturized Millimeter Wave Resonators with Self-Biased BaM Films **(11:30)**

Qian Gao, Yuanxun Ethan Wang
University of California Los Angeles, Los Angeles, CA

Miniaturized millimeter wave resonators that are based on the ferromagnetic resonance (FMR) of M-type barium hexagonal ferrite ($BaFe_{12}O_{19}$, BaM) films are proposed and simulated. The operating frequency can be up to 50 GHz without external biasing magnetic fields by virtue of the internal anisotropy field of BaM films. A novel stripline ridge structure is utilized to couple energy from transmission line to the ferromagnetic resonators. An equivalent circuit for such transmission line loaded ferrite resonator is used to optimize the design, and simulation results from full-wave simulator (HFSS) agree with circuit simulation results from ADS.

17.5: Magnetostatic Hexaferrites for Integrated mmWave Resonators and Filters **(11:50)**

Piotr Kulik, Augustine Kelty, David Connelly, Alexander Sokolov, Scott. Gillette
Metamagnetics, Inc., Marlborough, MA

Matthew Laurent, David Eaves, Nancy Lin, Dino Ferizovic
Northrop Grumman Corporation, Redondo Beach, CA

Magnetostatic surface wave (MSSW) mmWave filters are demonstrated here by utilizing hexaferrites $BaFe_{12}O_{19}$ (BaM) (3640G). Previously, MSW devices were only demonstrated on materials such as YIG (1780G) which require extremely high bias fields to operate in the mmWave range. Utilization of BaM allows for high frequency and the large anisotropy (H_A > 10,000 Oe) enables self-bias, hence requiring no external magnets. This work paves the path for leveraging novel ferrites in wideband mmWave AESAs that require small form factor.

LUNCH Supported by SkyWater Technology **(12:00–1:30)**
Golden State Ballroom

Session 18

RADIATION HARDENED BY DESIGN

Wednesday, 22 March / 10:30 – 11:50 am /
Town and Country Ballroom C

Chair: **Lloyd Massengill**
Vanderbilt University, Nashville, TN

18.1: A Radiation Hardened by Design FPGA with Distributed Single Event Upset Sensors, Embedded Error Handler, and 8 Mb Embedded MRAM Configuration Storage in 22 nm Bulk FinFET CMOS (10:30)

Onur Kibar, Oguz Atli, Prashanth Mohan, Ken Mai
Carnegie Mellon University, Pittsburgh, PA

Michael King
Sandia National Laboratory, Albuquerque, NM

This paper describes the design and testing of a radiation-hardened by design field-programmable gate array manufactured in a 22 nm bulk finFET process. The prototype FPGA employs SEU strike sensors, an embedded error handler, and an 8 Mb embedded MRAM configuration storage. The 33 × 33 tile FPGA is 2.09 mm × 1.79 mm, with each tile occupying 60.48 µm × 50.4 µm. The area, power, and delay overheads of adding the radiation hardening structures detailed in this paper are 23%, 5.8%, and 4.3%, respectively. Fig. 2 shows the strike sensor schematic. Heavy-ion single-event upset testing results are presented.

18.2: Reduce Your Design Costs by 10× for Robust Mixed Signal/Analog Design in Intel 16 and GF12 (10:50)

Thomas L. Wolf, Kent F. Smith, Jared Bytheway
Silicon Technologies, Inc., Salt Lake City, UT

State of the art electronics systems use sensors, batteries, wireless communications, video, audio, radar, GHz data transmission, clocks, and other analog circuits. The Intel 16 and GlobalFoundries 1 nm processes offer tremendous advantages for system performance. Building Rad Hard or Robust intergated circuits in the processes is possible. However, designing in the processes is complex, slow as there are over 40,000 design rules and complex modeling parameters the circuit designer and physical designer must handle. Using specialized tools such as TCAD is possible, but is slow and requires very specialized expertise to operate the tool. The ADONISTM Platform reduces the complexity of the design process by providing silicon proven design time and cost of state-of-the-art (SOTA) designs. An added feature is the ability to easily move your design from a standard commercial development to a Robust, Rad Hard integrated circuit quickly at low cost.

18.3: Achieving Rad-Hard FPGAs Using Standard Cell Libraries (11:10)

Greg Martin, Timothy Saxe, Tarachand Pagarani
QuickLogic Corporation, San Jose, CA

In this paper, we present the Australis (eFPGA IP Generator) Framework, which allows generation of Radiation Hardened eFPGA IP using a complete standard cell design approach, shortening its development and verification cycle.

18.4: A Radiation-Hardened by Design 15–22 GHz LC-VCO Charge-Pump PLL Achieving –240 dB FoM in 22 nm FinFET **(11:30)**

David Dolt, Samuel Palermo
Texas A&M University, College Station, TX

A radiation hardened PLL is designed in a 22 nm FinFET process achieving a 13–22 GHz frequency range and FOM of –237 dBc/Hz. This design incorporates radiation hardening techniques for both the analog and digital circuitry within the PLL. Moreover, this design will be tested at both the Texas A&M Cyclotron Institute to evaluate its robustness to single event effects (SEEs) and the TRIGA reactor to understand its degradation due to total ionizing dose (TID).

LUNCH Supported by SkyWater Technology **(12:00–1:30)**
Golden State Ballroom

Session 19

ADVANCES IN NEXT-GENERATION MICROELECTRONICS

Wednesday, 22 March / 10:30 – 11:50 am /
Town and Country Ballroom D

Chair: **Mona Massuda**
National Security Agency, Fort Meade, MD

Co-Chair: **Marcia Sawhney**
National Security Agency, Ft. Meade, MD

19.1: Advanced TCAD and EDA Tools in Support of VLSI Superconductor Electronics Design (10:30)

Robert Freeman, Jamil Kawa, Kishore Singhal
Synopsys, Inc., Mountain View, CA

As part of the IARPA sponsored SuperTools program targeting the SFQ5ee fabrication process at MIT Lincoln Laboratory, Synopsys is collaborating with industry and academia experts in the field of Superconductor Electronics (SCE) to develop a comprehensive set of physics based Technology Computer Aided Design (TCAD) tools for accurate modeling, and Electronic Design Automation (EDA) tools that enable the automation of digital SCE designs, thereby increasing the integration scale, efficiency, and manufacturability of these designs. The Synopsys team successfully completed the fifth and final phase of the IARPA sponsored project, offering demonstrations of significant advancement towards the program goals and metrics effecting RTL based VLSI designs utilizing Superconductor Electronics. Synopsys' Principal Investigators and Project Manager will present the full program efforts of Synopsys and that of our partners, our learnings, and our future direction.

19.2: Towards Low Profile Passive Magnetic Shielding for Cryogenic Electronics: Simulation and Material Characterization (10:50)

Sherman E. Peek, Mark L. Adams
Auburn University, Auburn, AL
and
Systems Visions LLC, Auburn AL

Siyuan Liu, Benjamin Pound, Robert Candler
University of California Los Angeles, Los Angeles, CA

Harshil Goyal, Michael C. Hamilton
Auburn University, Auburn, AL

George Hughes
Systems Visions LLC, Auburn AL

19.3: Optimizing System-on-Chip Designs Using AI (11:10)

Manpreet Singh, Nitin Garg
Synopsys, Inc., Mountain View, CA

Finding the optimal System-on-Chip (SoC) design parameters for a specific software application is a multi-objective design optimization problem, where competing design vectors are PASS – Power, Area, Speed (Performance) and Security. Today's state-of-the-art method to do so is user driven simulation-based architecture exploration and optimization which is very tedious and manual intensive task. In this paper, we propose a novel Artificial Intelligence (AI) based approach which finds out the optimal set of SoC design parameters automatically by efficiently exploring the vast design space. Novelty of this solution lies in the fact that it is faster and at least as optimal as than the current approach.

19.4: Prolegomena to Any Future Device Physics (11:30)

Adam L. Friedman, Aubrey T. Hanbicki
Laboratory for Physical Sciences, College Park, MD

For the last 60 years, advances of computing platforms have been driven by Moore's law. The reluctant consensus is that Moore's law will disappear. The end of this trend has been thwarted by advances in many aspects of the computing ecosystem including materials improvements, device design, device/circuit "cleverness," and architectural innovations. While many have argued the impending doom of Moore's law is imposed by atomic length scales, quantum processes, and energy consumption limits, we contend that Moore's law must be jettisoned for a different reason: Words matter. Even those adamantly declaring the end of Moore's law still use the language of Moore's law, inhibiting progress. We suggest a more outwardly focused perspective and a shift in language to a regime we coin the Feynman Mandate. In this perspective we outline the issues with the continued use of Moore's law as well as a prescription of transitioning to a new lexicon.

LUNCH Supported by SkyWater Technology (12:00–1:30)
Golden State Ballroom

Session 20

ADVANCES IN ELECTRONIC MATERIALS AND PROCESSES

Wednesday, 22 March / 10:30 am – 12:10 pm / Palms Room 1-3

Chair: **Tony Ivanov**
Army Research Laboratory, Adelphi, MD

Co-Chair: **Nian Sun**
Northeastern University, Boston, MA

20.1: **Direct Write Processing of Low Loss Polymeric Dielectrics for Heterogeneous Integration** **(10:30)**

Fahima Ouchen, Laura Davidson
KBR, Defense and Intel, Dayton, OH

Ahsan Mian, Lucas Clark
Wright State University, Dayton, OH

Emily Heckman, Thomas Taylor, Jeffrey Massman
Air Force Research Laboratory, Wright-Patterson AFB, OH

The development of direct write fabrication techniques for depositing low loss and low k dielectric materials is demonstrated for potential applications in multifunctional redistribution layers (RDLs) for fan-out/in interconnects in PCB heterogeneous integration. The polymers were selectively deposited as the dielectric interlayer on a PCB between an RF and DC signal crossover using the direct write technique of aerosol jet printing. The characterization and performance of the dielectric materials are reported, and the printed crossovers are compared to their commercial counterparts.

20.2: **Silica Based Inorganic Composite for Heterogenous Integration** **(10:50)**

Ryan Benz, Bradley Duncan, Devon Beck, Connor Belanger, Matt Ricci, Al Cabral, Melissa Smith
Massachusetts Institute of Technology, Lexington, MA

Currently, there is strong demand across government and commercial sectors for high densification of microelectronics. Wafer level packaging and heterogenous integration strategies provide a potential solution for tighter integration and higher densification of electronics. However, conventional packaging materials are limiting the ability of these techniques to address the advanced needs of microelectronics fabrication. These limitations predominately stem from the organic-based chemistries that traditional packaging materials are composed of. These organic-based packaging materials have high coefficients of thermal expansion, complex deposition processes, and have low compatibility with further microfabrication steps. Due to the organic nature of these materials, they also outgas, have low thermal stability, and poor mechanical stability. In this work, we describe a new inorganic-based silicate composite material that can be deposited in thick layers (10–20 µm) through air spray, casting, and spin coating. This material is synthesized with clean room grade starting materials ensuring insertion into exist microfabrication process flows. After cure, this material has thermo-mechanical, chemical and RF properties comparable to a quartz silica. Broadly, we find that this material will be of significant use for high density CMOS compatible systems, and also specifically high-density phased arrays.

20.3: Additive Manufacturing of Graphene Composite Conductors and Particle-less Metallic Inks (11:10)

Luke Lyle, Lach Peeke, Isaiah Adu, Joshua Fox, Kristoffer Greenert, David Snyder
Pennsylvania State University – Applied Research Lab, State College, PA

Additive manufacturing (AM) has made great strides in development over the last few decades. Through novel manufacturing technologies to innovative material systems, these technologies have enabled the production of new and exciting products. Success of AM on the commercial scale hinges on its adoption into manufacturing for complex geometry assemblies. The packaging and manufacturing of thin and flexible electronics provides a proving ground for the combination of novel materials and cutting edge AM hardware to produce parts capable of changing how we engage with electronics. Research presented showcases the Electronics and Materials Devices Department (EMDD) at the Applied Research Lab (ARL) at Penn State working on developing highly conductive graphene composite conductors and particle-less metal inks. This research has been geared towards high frequency antennas on flexible and stretchable substrates.

20.4: Additive Manufacturing of Multimaterial Radiation Shielding (11:30)

Bradley Duncan, Devon Beck, Ryan Benz, Paul Miller, Salvatore Di Cecca, Melissa Smith
Massachusetts Institute of Technology, Lexington, MA

The harsh radiation environment of space induces the degradation and malfunctioning of electronic systems. Current approaches for protecting these microelectronic devices are generally limited to attenuating a single type of radiation or require only selecting components that have undergone the intensive and expensive procedures to be radiation-hard by design or by process. We describe an alternative fabrication strategy to manufacture multimaterial radiation shielding via the direct ink writing of custom composites. The additively manufactured shields were shown to be capable of attenuating multiple species of radiation by tailoring the composition and architecture of the printed composite materials. This generalized method offers a promising approach for protecting any commercially available microelectronic system from radiation damage and we anticipate this vastly enhance the capabilities of future satellites and space systems.

20.5: A Semiconductor Foundry in a Box: Additive Manufacturing of Electronics and Heterogenous Integration for Advanced Packaging (11:50)

Ahmed Busnaina, Sudhir Jain
Nano OPS, Inc., Burlington, MA

A new technology that enables the additive manufacturing of nano and microelectronics, electronic components, and RDL while reducing the cost by 10–100 times and can print 1000 faster and 1000 smaller structures than ink-jet-based printing. The nano and microscale printing platform enables the heterogeneous integration of interconnected circuit layers (like CMOS) of printed electronics and sensors at ambient temperature and pressure on rigid or flexible substrates. Printed applications were demonstrated such as transistors, inverters, diodes, and logic gates, and displays at the micro and nanoscale using inorganic and organic materials will be presented. The capability of printing RDL, passive and active components monolithically allows the reduction of a board (such as an IOT board) to be within a few mm of the original IC (chip) footprint. Additionally, the number of parts used will be reduced by more than 75%, and the footprint by more than 90% to reduce size and weight.

Panel Discussion

SIFTING THROUGH THE CHAOS: ARE BEST PRACTICES ACHIEVABLE?

Wednesday, 22 March / 10:30 am – 12:10 pm / Palms Room 4-6

LUNCH Supported by SkyWater Technology (12:00–1:30)
Golden State Ballroom

Session 21

ULTRA-WIDE BANDGAP DEVICES AND H2

Wednesday, 22 March / 1:30 – 3:10 pm /
Town and Country Ballroom A

Chair: **Thomas Kazior**
Raytheon Technologies, Goleta, CA

21.1: **Engineering Heterogeneous III-V/III-N Interfaces for High-Power Heterojunction Bipolar Transistors** **(1:30)**

Rohan Sengupta, Brian Little, Keith Markham, Shane Stein, Tim Day, Zlatko Sitar, Fred Kish, Spyridon Pavlidis
North Carolina State University, Raleigh, NC

Seiji Mita, Zlatko Sitar
Adroit Materials, Inc., Cary, NC

The use of heterogeneous heterojunctions for HBTs expands the device design space and offers the opportunity to address the performance limitations of conventional semiconductor technologies. Here, we present III-V/III-N diodes using a novel heterogeneous integration process. We report on the electrical behavior of these diodes, including a minimum interface trap density that is more than 50× smaller than the sheet charge density of the corresponding HBT base layer. Limited details are provided in this abstract due to a pending patent application.

21.2: **Heterogeneous Heterostructure Transfer Bipolar Transistor** **(1:50)**

Clincy Cheung, Vincent Gambin, Aaron Oki
Northrop Grumman Space Systems, Redondo Beach, CA

Donghyeok Kim, Jiarui Gong, Qiming Zhang, Haris Naeem Abbasi, Hokyung Jang, Jie Zhou, Daniel Vincent, Zhenqiang (Jack) Ma
University of Wisconsin-Madison, Madison, WI

Today's candidate ultra-wide bandgap (UWBG) semiconductor material systems come with significant tradeoffs in properties and performance which can limit their adoption in RF power electronics. This paper reports on our Heterogeneous Heterostructure (H2) transfer bipolar transistor (XBT) approach enabling materials with largely different atomic spacing and mismatched crystal structures to be used within the intrinsic device structure. This process can form device structures never before possible using traditional hetero-epitaxy techniques. A ScAlN UWBG collector is combined with a GaAs base and AlGaAs emitter using atomic layer deposition (ALD) "grafting" technology developed by the University of Wisconsin-Madison. This results in an optimal base-collector junction for electron flow with a minimal interface trap density. The UWBG collector provides high breakdown and high saturated velocity while the smaller gap GaAs can be heavily p-type doped with minimal resistance. This new structure results in a high-performance bipolar RF device far exceeding existing solutions.

21.3: Progress Towards AlN Channel UWBG HEMT Heterostructures for RF Applications **(2:10)**

Virginia Wheeler, Neeraj Nepal, Matthew Hardy, Andrew Lang, Brian Downey, David Meyer
U.S. Naval Research Laboratory, Washington, DC

Eduardo Chumbes, John Logan, Lovelace Soirez
RF Components, Raytheon Technologies, Andover, MA

Jeffrey LaRoche
Raytheon Missiles & Defense, Tewksbury, MA

21.4: Cubic Boron Nitride / Diamond Heterojunctions for Next Generation RF Electronics **(2:30)**

D. Meyer, D. Storm, N. Nepal, A. Lang, J. Champlain, B. Downey, V. Gokhale, V. Wheeler
U.S. Naval Research Laboratory, Washington, DC

M. Hollis, B. Zhang, M. Geis, D. Calawa, J. Mallek, J. Daulton, A. Melville, M. Polking, G. Turner
MIT Lincoln Laboratory, Lexington, MA

21.5: Growth Development of Ultra-wide Bandgap AlN/GaN Digital Alloys for Lateral RF Devices **(2:50)**

Shin Mou, Alex Chaney, Adam T. Neal, Tadj Asel, Dave Turner, Cindy Bowers, Yunjo Kim, Joshua Melnick
Air Force Research Laboratory, Materials & Manufacturing Directorate, Wright-Patterson AFB, OH

Henry Aller, Samuel Graham Jr.
University of Maryland, College Park, MD

Patrick Hopkins
University of Virginia, Charlottesville, VA

BREAK Supported by Flex Logix Technologies **(3:10–3:30)**
Golden State Ballroom

Session 22

FPGA SECURITY

Wednesday, 22 March / 1:30 – 3:10 pm /
Town and Country Ballroom B

Chair: **Mona Massuda**
National Security Agency, Fort Meade, MD

22.1: **Starbleed Effects and Countermeasures for 7-series and Ultrascale(+) AMD-Xilinx FPGAs** **(1:30)**

Christopher Sozio, Adam Duncan
NAVSEA Crane, Crane, IN

22.2: **Integrity and Assurance Tools Targeting FPGA Hard IP Block Bitstream Undocumented Functionality** **(1:50)**

Andrew G. Schmidt, Benedict Reynwar, Kellie Canida, Matthew French
University of Southern California, Arlington, VA

22.3: **MicroBitstreams: Reducing Configuration Time of Encrypted Bitstreams** **(2:10)**

Christopher Sozio, Daniel Hansen, Adam Duncan
NAVSEA Crane, Crane, IN

Grant Skipper, Andrew Lukefahr
NAVSEA Crane, Crane, IN
and
Indiana University, Bloomington, IN

22.4: **Efficient Porting of FPGA Independent Testing Within and Across Vendors** **(2:30)**

Travis Haroldsen, Ting-Yuan Sung, Osaze Shears
University of Southern California, Arlington, VA

Dallon Glick, Jay Danner
Georgia Institute of Technology

22.5: **FPGA-Based Verification and Profiling of an Optimized seL4 OS for Resource Constrained Applications** **(2:50)**

Jeremy Porter, Sayed Elgendy, Eslam Tawfik
Ohio State University, Columbus, OH

Jeff Durrum
Booze Allen Hamilton, Beavercreek, OH

The research presented in this paper is an exploration of minimal RISC-V architectures. A resource constrained RISC-V SoC implementations is considered. The goal is to provide a resource usage profile on an SoC with an OS. A modified operating system is used to run benchmarking applications to determine processing time and power. This custom seL4 moves the payload to a lower memory address and reduces the default page table size from 2 MB to 4 KB. These modifications along with others reduces the memory footprint to below 2 MB. As a result of this work, a comparison of common RISC-V architectures are compared with respect to resources required (number of gates), power consumption, and processing time. The previously presented verification framework is implemented and extended to consider multiple architectures as well as benchmarking applications.

BREAK Supported by Flex Logix Technologies **(3:10–3:30)**
Golden State Ballroom

Session 23

DATA PROTECTION IN VIRTUAL ENVIRONMENTS (DPRIVE)

Wednesday, 22 March / 1:30 – 3:10 pm /
Town and Country Ballroom C

Co-Chair: **Johnny Marsh**
DARPA, Arlington, VA

23.1: **TREBUCHET: Fully Homomorphic Encryption Accelerator for Deep Computation** **(1:30)**

David Bruce Cousins, Yuriy Polyakov, Ahmad Al Badawi
Duality Technologies, Hoboken, NJ

Matthew French, Andrew Schmidt, Ajey Jacob, Benedict Reynwar, Kellie Canida, Akhilesh Jaiswal, Clynn Mathew
University of Southern California, Arlington, VA

Homer Gamil, Negar Neda, Deepraj Soni, Michail Maniatakos, Brandon Reagen
New York University, New York City, NY

Naifeng Zhang, Franz Franchetti
Carnegie Mellon University, Pittsburgh, PA

Patrick Brinich, Jeremy Johnson
Drexel University, Philadelphia, PA

Patrick Broderick, Mike Franusich
SprialGen, Inc., Pittsburgh, PA

Bo Zhang, Zeming Chen, Massoud Pedram
University of Southern California, Los Angeles, CA

Secure computation is of critical importance anywhere personally identifiable information is accessed and in many DoD applications. Traditional security techniques require data to be decrypted before performing any computation, leaving it vulnerable to attacks. Fully Homomorphic Encryption (FHE) keeps the data encrypted during computation and secures the results, even in untrusted environments. However, FHE requires a significant amount of computation to perform the equivalent unencrypted operations. The goal of the TREBUCHET project is to accelerate FHE computation to within 10× of traditional processing. We accelerate the major secure standardized FHE schemes (BGV, BFV, CKKS, FHEW, etc.) at >=128-bit security while integrating with the open-source OpenFHE library. We utilize a novel tile-based chip design with highly parallel ALUs optimized for vectorized 128b modulo arithmetic. The TREBUCHET co-processor design provides a highly modular, flexible, and extensible FHE accelerator for easy reconfiguration, deployment, integration and application on other hardware form factors.

23.2: **BASALISC: Programmable Asynchronous Hardware Acceleration for BGV and CKKS Fully Homomorphic Encryption** **(1:50)**

Daniel Wagner, Ben Selfridge, David W. Archer
Galois, Inc., Portland, OR

Robin Geelen, Michiel Van Beirendonck, Hilder V. L. Pereira, Ingrid Verbauwhede, Frederik Vercauteren
KU Leuven, Leuven, Belgium

Tynan McAuley, Georgios D. Dimou
Niobium Microsystems, Inc., Dayton, OH

23.3: Intel® HERACLES: Homomorphic Encryption Revolutionary Accelerator with Correctness for Learning-oriented End-to-End Solutions **(2:10)**

Chris Wilkerson, Sachin Taneja, Raghavan Kumar, Sanu Mathew, Jeremy Casas, Jin Yang, Michael Steiner, Huijing Gong, Wen Wang, Duhyeong Kim, Ro Cammarota
Intel Labs, Santa Clara, CA

Poornima Lalwaney, Adish Vartak, Vasantha Srirambhatla, Sandeep Jain, AppaRao Ch
Intel Corporation, Santa Clara, CA

Fully Homomorphic Encryption (FHE) enables software applications to process encrypted data without decryption. Processing encrypted data has the potential to elevate the bar of confidentiality in existing security solutions by both protecting data owner's privacy and greatly reducing the risk of third-party data leakage. Unfortunately, FHE in software comes with prohibitive overheads, increasing latency by as much as six orders of magnitude on existing CPUs. Intel® HERACLES is a new type of near memory computer architecture with tightly connected functional units and distributed memory, that bridges the performance gap, enabling the benefits of FHE deployment in next generation security solutions.

23.4: HEM: Memory-based Acceleration for Fully Homomorphic Encryption **(2:30)**

Minxuan Zhou, Pranav Gangwar, Yujin Nam, Arpan Dutta, Tajana Rosing
University of California, San Diego, San Diego, CA

Chris Wilkerson, Rosario Cammarota
Intel Labs, Hillsboro, OR

Saransh Gupta
IBM Research, Yorktown, NY

Fully Homomorphic Encryption (FHE) is a promising technique that enables arbitrary computations on encrypted data, securing many emerging cloud-based applications. However, FHE introduces significant computation overhead, which is usually several orders of magnitude slower than computation on plain data due to the explosion of both data and computation after encryption. Existing accelerators for FHE rely on large on-chip scratchpads to match the throughput of on-chip processing elements. However, the performance of these accelerators is still bounded by the off-chip memory bandwidth. The memory-bound issue is challenging because further increasing the on-chip scratchpad and memory bandwidth is not area- and energy- efficient. In this work, we propose a new FHE accelerator based on memory-based computing in emerging DRAM. The proposed memory-based accelerator exploits the highly parallel in-memory operations with specialized near-memory components to optimize the computation and data transfer patterns of FHE applications. In addition to the hardware design, we formulate the problem of mapping FHE programs onto the memory-based accelerator and propose a compiler-level optimization framework to generate an efficient data layout. We evaluate the efficiency of the proposed design on widely-used FHE applications for machine learning. Our evaluation shows that the proposed accelerator can provide up to 8.29× more throughput than state-of-the-art FHE accelerators while consuming 2.83× less power and 3.84× less chip area.

23.5: Test and Evaluation for DARPA DPRIVE Program (2:50)

John G. Wohlbier, Drew J. Dolgert
Advanced Computing Lab, AI Division, CMU-SEI, Pittsburgh, PA

Performers in the DARPA Data Protection in Virtual Environments (DPRIVE) program are designing hardware to accelerate algorithms evaluated with Fully Homomorphic Encryption. With current CPU technology it takes approximately 10^6 times longer to train a 7-layer CNN on BGV encrypted data than training the same CNN on unencrypted data. The DPRIVE program seeks to create custom hardware that can reduce this time difference by five orders of magnitude. CMU-SEI is performing test and evaluation of performer designs on behalf of DARPA. Performing a fair comparison of newly designed hardware from multiple performer teams presents several challenges. The primary difficulties come from the inherent differences in the performer ISAs and performer workload implementation choices. We have developed a methodology whereby comparisons are possible. We provide details of the workload that is used as the basis of comparison, the method of communicating the workload to performers, and anonymized performer results.

BREAK Supported by Flex Logix Technologies (3:10–3:30)
Golden State Ballroom

Session 24

QUANTUM TECHNOLOGIES

Wednesday, 22 March / 1:30 – 3:10 pm /
Town and Country Ballroom D

Chair: **Michael Lovellette**
The Aerospace Corporation, Chantilly, VA

Co-Chair: **Barry Treloar**
Strategic Systems Programs, Washington, DC

24.1: Metrics for Non-linear Response in Rydberg Quantum RF Receivers: Two-tone Testing and Intermodulation Distortion **(1:30)**

Luís F. Gonçalves, Rémy Legaie, Georg Raithel, David A. Anderson
Rydberg Technologies, Inc., Ann Arbor, MI

Non-linear responses and intermodulation distortion behavior of an RF receiver system are of critical importance to the receiver's spur-free dynamic range and tolerance to unwanted interfering signals. We report on the measurement and characterization of non-linear behavior and spurious response of a quantum RF aperture/receiver based on Rydberg atoms. Single-tone and two-tone tests are performed on a Rydberg atomic heterodyne receiver using two-photon EIT in a room-temperature cesium vapor. For a predetermined set of atomic receiver parameters and using near-resonant Autler-Townes transitions at RF carriers in the SHF band, we measure a spur-free dynamic range, P1dB compression, and third-order (IP3) intercept. We find that under suitable operating conditions atomic receivers can exhibit a suppression of harmonic and inter-modulation distortion compared to classical receiver mixers, and can be characterized by unique RF signatures in their non-linear response that may be exploited in applications.

24.2: A Superconducting Qubit Foundry at MIT Lincoln Laboratory **(1:50)**

Cyrus F. Hirjibehedin, Jeffrey Knecht, Kate Azar, Bethany M. Niedzielski, Mollie E. Schwartz
Massachusetts Institute of Technology, Lexington, MA

24.3: Mitigation of Quantum Measurement Errors with Distribution-based Learning **(2:10)**

Zachery Utt, Daniel Volya, Prabhat Mishra
University of Florida, Gainesville, FL

Quantum measurement is one of the critical steps in quantum computing that determines the probabilities associated with qubit states after conducting a computation. Since real quantum computers are prone to noise, a major challenge in quantum measurement is how to correctly interpret the noisy data from a quantum computer. While there are promising classification based solutions, they either produce incorrect results (misclassify) or require many measurements (expensive). In this paper, we present an efficient technique to estimate a qubit's state through analysis of probability distributions of post-measurement data. Specifically, we estimate the state of a qubit using cumulative distribution functions to compare the measured distribution of a sample with the distributions of basis states 0 and 1. Our experimental results demonstrate a drastic reduction (78%) in single qubit readout error and a reduction (12%) when used to boost existing multi-qubit discriminator models.

24.4: A Quantum Algorithm for Graph Clustering (2:10)

Daniel Volya, Prabhat Mishra
University of Florida, Gainesville, FL

Spectral graph partitioning is a well known technique to estimate clusters in undirected graphs. Recent approaches explored efficient spectral algorithms for directed and mixed graphs utilizing various matrix representations. Despite its success in clustering tasks, classical spectral algorithms suffer from a cubic growth in runtime. In this paper, we propose a quantum spectral clustering algorithm for discovering clusters and properties of mixed graphs. Our experimental results based on numerical simulations demonstrate that our quantum spectral clustering outperforms classical spectral clustering techniques. Specifically, our approach leads to a linear growth in complexity, while state-of-the-art classical counterpart leads to cubic growth. In a case study, we apply our proposed algorithm to preform unsupervised machine learning using both real and simulated quantum computers. This work opens an avenue for efficient implementation of machine learning algorithms on directed as well as mixed graphs by making use of the inherent potential quantum speedup.

24.5: Designing Complex Mathematical Functions using Quantum Hardware (2:30)

Chao Lu, Amisha Srivastava, Kanad Basu
University of Texas at Dallas, Richardson, TX

Quantum computing has been shown to provide exponential acceleration over classical computers in various domains, including machine learning, cryptography, and molecular simulation. In this paper, we propose several approaches to design complex quantum arithmetic circuits to facilitate homomorphic encryption and post quantum cryptography encryption algorithms. Specifically, we focus on Number Theoretic Transform (NTT) and Learning With Errors (LWE) arithmetic circuits. To this end, we propose the design and verification of these algorithms using quantum hardware.

Session 25

THERMALLY HARDENED ELECTRONICS

Wednesday, 22 March / 1:30 – 3:10 pm / Palms Room 1-3

Chair: **Benjamin Griffin**
DARPA, Arlington, VA

Co-Chair: **Rocco Radoslav**
ECS Federal, Arlington, VA

25.1: Scalable Electronics for Extreme Environments: Lessons Learned from Testing to the Hypersonic Temperature Range **(1:30)**

A. Matt Francis, Jacob P. Kupernik, James Holmes, Nicholas J. Chiolino, Sonia Perez
Ozark Integrated Circuits, Inc., Fayetteville, AR

The operation of electronics in extreme environments (elevated temperature, pressure, and vibration) is required to digitize the next frontier of many critical, defense and energy applications. From turbine engines to molten salt reactors, electronics that can operate in the extreme conditions remain lacking. Through targeting potential hypersonic and turbine engine profiles, electronics from 200 °C to 800 °C have been identified as an area requiring unique solutions that are more complicated than simple "uprating" of standard integrated circuit and packaging technologies. In this work, a scalable approach to solving these problems will be presented, based on lessons learned from evaluating operating electronics to 800°C. The identification of areas requiring further investment from the electronics ecosystem are also addressed.

25.2: The Next Generation of High-Temperature Integrated Circuits with SiC CMOS **(1:50)**

Zeynep Dilli, Neil Goldsman, Chris Darmody, Akin Akturk, Usama Khalid, Mitchell Gross, Ryan Purcell, Ethan Mountfort, Yekta Kamali
CoolCAD Electronics, College Park, MD

Benjamin Griffin
DARPA, Arlington, VA

25.3: Manufacturability of All-Implant SiC JFET for High Temperature Applications **(2:10)**

Amrita Masurkar, Isaac Wildeson, Bill Zivasatienraj, David Brown, Puneet Srivastava, Louis Mt. Pleasant, Louis Lanzerotti
BAE Systems, Inc., Nashua, NH

Mark Fanton, Randal Cavalero, Luke Lyle, David Snyder
Pennsylvania State University, University Park, PA

There is a growing need within the defense industrial base for microelectronics that can operate at temperatures beyond 300 °C. Accordingly, we present the development of a manufacturable, SiC JFET capable of sub-10 V threshold voltage and operation well above 300 °C. Both normally-on and normally-off devices are discussed. The benefits of the process include low operating voltages and complementary logic. A discussion is included on key materials and processes for realizing SiC complementary logic and the challenges of developing a high manufacturing readiness level process using existing domestic semiconductor manufacturing resources.

25.4: High Temperature Studies of 140 nm T-gate AlGaN/GaN HEMT Devices **(2:30)**

Ahmad Islam, Dennis E. Walker Jr., Nicholas C. Miller, Matt Grupen, Kyle J. Liddy, Antonio Crespo, Gary Hughes, Kelson D. Chabak, Andrew J. Green
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, Dayton, OH

Adam T. Miesle, Nicholas P. Sepelak
KBR, Inc., Beavercreek, OH

Hanwool Lee, Wenjuan Zhu
University of Illinois, Urbana, IL

We studied high temperature (up to 500 °C) operation of AlGaN/GaN high-electron mobility transistors (HEMT). Measurements showed a reduction in gate modulation of the drain current due to an increase in gate leakage. Devices also exhibited a ~85% reduction in transconductance, a reduction in threshold voltage, and an increase in series resistance at a higher measurement temperature. At 500 °C, the devices exhibited continuous loss of gate modulation, which led to an eventual failure of devices potentially due to diffusion of gate metals into the device.

25.5: High Temperature Modeling of Commercial GaN HEMTs Using an Enhanced MVSG Framework **(2:50)**

John Niroula, Qingyun Xie, Mengyang Yuan, Pradyot Yadav, Tomás Palacios
Massachusetts Institute of Technology, Cambridge, MA

Darren Brock, Jonathan Nichols, John J. Callahan
Lockheed Martin Corporation, Billerica, MA

GaN transistor technology is a promising candidate for electronics at extreme temperatures that will allow the exploration of energy-rich geothermal wells, flight of hypersonic aircrafts, and space exploration of the surface of Venus. Here we characterize the DC performance of a commercial discrete GaN HEMT device from 25 °C–300 °C. Furthermore, we enhanced the MIT Virtual Source GaN FET (MVSG) model to account for temperature dependent leakage current, subthreshold swing, and contact resistance. This model was used to estimate the large signal loadpull performance at elevated temperatures, as the commercially available model was not designed to run at such elevated temperatures.

BREAK Supported by Flex Logix Technologies (3:10–3:30)
Golden State Ballroom

Panel Discussion

PERSPECTIVES ON COMPUTATIONAL METHODS FOR RADIATION HARDNESS QUALIFICATION

Wednesday, 22 March / 1:30 – 3:10 pm / Palms Room 4-6

BREAK Supported by Flex Logix Technologies (3:10–3:30)
Golden State Ballroom

Session 26

WARP II

Wednesday, 22 March / 3:30 – 4:50 pm /
Town and Country Ballroom A

Chair: **David Abe**
DARPA / Microsystems Technology Office, Arlington, VA

Co-Chair: **Andrew Wegener**
Air Force Research Laboratory, Wright-Patterson AFB, OH

26.1: Hybrid Analog Cancellation Filter (3:30)

David Landon, Scott Hinton
L3Harris Technologies, Salt Lake City, UT

Alyosha Molnar, Alyssa Apsel
Cornell University, Ithaca, NY

Dan Bliss, Carl Morgenstern
Arizona State University, Tempe, AZ

We present integrated hardware and algorithmic developments for a wide-band self-interference cancellation (SIC) system for multi-antenna wireless systems. The canceller circuit takes in a reference signal, coupled from the radio's transmitter path, convolves that signal with a 64-tap analog FIR filter and subtracts the result from the receiver path. Cancellation and receive paths are combined in an inductor-capacitor (LC) delay line, which provides tap delays for the highest power, relatively low-delay taps, and absorbs the significant parasitics of the canceller hardware. Longer delay taps, which are assumed to be weaker, are implemented with a switched-capacitor delay system which feeds into the same LC combiner. We have also developed algorithms to discover an appropriate, sparse set of tap weights for any given TX-to-RX coupling scenario, while leveraging and compensating for the properties of the hardware, such as the need for strictly constrained non-negative taps.

26.2: A Hybrid Time-Domain/Frequency-Domain RF Self-Interference Canceller (3:50)

Mark D. Hickle, Stephen Mroz, Jeffrey Feigin
BAE Systems, Merrimack, NH

Sastry Garimella, Harish Krishnaswamy
Columbia University, New York, NY

26.3: Photonic-Acoutic Assisted Wideband Self Interference Cancellation **(4:10)**

Mertcan Erdil, Izhar FNU, Roy H. Olsson III, Firooz Aflatouni
University of Pennsylvania, Philadelphia, PA

Self-interference, as an important challenge in full-duplex transceivers, can be suppressed by injecting a small fraction of the TX output to the RX input after phase, delay, and amplitude adjustments. For wide band RF transceivers, a low-loss, highly-linear tapped delay line, tunable over tens of nano seconds, is an essential component in such a self-interference cancellation scheme. Low acoustic wave velocity in Si makes acoustic delay lines a good candidate to realize low-loss multi nano second delay lines, where bi and unidirectional acoustic transducers, converting the TX electrical output to acoustic waves, can be realized using aluminum scandium nitride (AlScN) as the piezoelectric material. We are developing an array of amplitude adjustable tunable tapped delay lines, where course delay is realized through acoustic delay lines and fine tunable delay as well as amplitude control are realized in the optical domain.

26.4: A 0.2–2 GHz RF Delay Element Achieving 2.55–448.6 ns Programmable Delay Range **(4:30)**

Travis Forbes, Benjamin Magstadt, Jesse Moody, Justine Saugen, Andrew Suchanek, Spencer Nelson
Sandia National Laboratories, Albuquerque, NM

Simulation of radar returns in electronic warfare (EW) and radar test devices, as well as filters for full-duplex systems desire hundreds of ns of programmable broadband RF delay in the signal path to simulate large distances in EW and radar testers, and for object reflection cancellation in full-duplex. However, low-power programmable RF delay has been limited to ones of ns in prior works. In this work, we present a 0.2–2 GHz digitally programmable RF delay element based on a time-interleaved multi-stage switched-capacitor approach. The delay element was implemented in a 45 nm SOI CMOS process and achieves a 2.55–448.6 ns programmable delay range with <0.12% delay variation across 1.8 GHz bandwidth, 330 ns/mm^2 area efficiency, and maintains delay performance across temperature variation.

Wednesday Evening Social at San Diego Zoo **(7:30–9:30)**

Session 27

SIGNAL CONVERSION CIRCUITS AND TECHNIQUES

Wednesday, 22 March / 3:30 – 5:10 pm /
Town and Country Ballroom B

Chair: **Peter Buxa**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Christal Gordon**
Booz Allen Hamilton, Arlington, VA

27.1: **An Optimized Training Process for Nonlinear Equalization** **(3:30)**

J. Landon Garry, Alexander Adeleye, Katelyn Hampel, Zachary Peck
Johns Hopkins University Applied Physics Laboratory, Laurel, MD

27.2: **A Gallium Nitride (GaN) Nyquist-Folding RF Sampler for Compressed Sensing Applications** **(3:50)**

Samantha McDonnell, Lauren Pelan, William Gouty, Tony Quach
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

27.3: **Cognitive Spectrum Optimization** **(4:10)**

Scott R. Velazquez, Brennan Eveland
TM Technologies, Inc., San Diego, CA

A suite of novel, complementary technologies is used to enable dynamic, cognitive optimization of communications spectrum usage in congested and dynamic radio frequency environments. The term Transpositional Modulation (TM) is used to refer to this suite of technologies. TM increases data rates of traditional systems and provides obfuscated communications without using additional spectrum or interfering with the original waveform. Adaptive spectral monitoring is used to identify and exploit room under spectral emissions masks to add additional, non-interfering channels of communication; digital pre-distortion linearization techniques increase the room under the mask by removing intermodulation distortion. In addition, self-interference cancellation techniques allow overlaying additional communications to existing systems in the same frequency band at the same time. Customized coding and encryption techniques enhance the reception of TM signals and provide secure communications. Hardware test results with a modern software defined radio platform confirm increases in data rate by over 50%.

27.4: A Compact and Efficient 12-GSps RF-Sampling Analog Front End for Software Defined Radio in 16 nm **(4:30)**

Mikko Waltari, Costantino Pala, Pedro Paro, Sunit Sebastian, Devon Thomas, Anders Ihlstrom, Narek Rostomyan, George Baird, Dave Smith, Mike Kappes
IQ-Analog Corporation, San Diego, CA

A 12-GSps transceiver front end features direct RF sampling capability up to 8 GHz signal frequency. Implemented in 16nm FinFET technology, the block consists of a dual ADC, a dual DAC, a PLL, and supporting circuitry. This compact and power efficient module enables next generation RF transceivers based on software defined radio architecture serving various applications. It is well suited for phased array antenna systems utilizing element level digital beam forming.

27.5: A Scalable Resolution and Frequency SAR ADC with State-of-the-Art Figure of Merit Across 8–10 b and 12.5-to-734 MS/s in 22 nm FDSOI **(4:50)**

Mo'men Mansour, Michael Kines, Sam Ellicott, Trevor Dean, Shane Smith, Waleed Khalil
The Ohio State University., Columbus, OH

High efficiency ADCs are designed to operate over narrow supply, resolution, and frequency ranges. This work focuses on a scalable ADC that can accommodate a wide range of standards through variable sampling rate, precision, and supply voltage while maintaining high efficiency. The proposed ADC utilizes a fully dynamic flexible SAR architecture with a wide range of supply adaptation to acclimate wide range of sampling rates. Furthermore, it also incorporates a resolution scalable DAC, comparator, and SAR logic to attain efficient conversion at multiple resolutions. The measured prototype achieves sampling rates from 12.5 to 734 MS/s at 8–10-bit resolution, with record tracking FOM of 0.83 to 5.87 fJ/c-s.

Wednesday Evening Social at San Diego Zoo **(7:30–9:30)**

Session 28

DESIGN OF SECURE SYSTEMS

Wednesday, 22 March / 3:30 – 5:10 pm /
Town and Country Ballroom C

Chair: **Shawn Fetterolf**
Intel Federal, LLC, Santa Clara, CA

28.1: **Secure AI Hardware By Design: From Cryptographic Proofs to Silicon Tape-Out** **(3:30)**

Anuj Dubey, Aydin Aysu
North Carolina State University, Raleigh, NC

Rosario Cammarota
Intel Labs, San Diego, CA

Machine learning (ML) and artificial intelligence (AI) applications are increasingly being used in critical cyberinfrastructure. Therefore, trusted execution with AI/ML hardware is becoming a fundamental requirement for next-generation applications. Specifically, the data privacy and intellectual property protection of AI/ML models is of primary importance. New attacks have emerged that can steal this information through side-channels via observing unintentional hardware leakages such as power consumption, electromagnetic radiation, and execution time. Although such attacks and related defenses were known for cryptographic applications, their extensions to AI/ML frameworks are unknown and non-trivial. In our research, we have demonstrated new side-channel attacks on AI/ML hardware and proposed novel defenses to mitigate the vulnerability. Our solution is full stack—it encompasses all abstraction levels starting from theoretical proofs of security all the way down to a silicon chip tape-out. We developed cryptographic proofs for security, mapped those provable systems into custom hardware units, integrated them into a RISC-V architecture and microarchitecture, enhanced the compiler flow for custom instruction integration, implemented and taped-out the design on a 130 nm technology node, and demonstrated both practical and theoretical security.

28.2: **Cybersecurity of System-on-Chip Based Multi-Drone Systems** **(3:50)**

Michael Vai, Alice Lee, Karen Gettings, Matthias Beebe, Paul Monticciolo
MIT Lincoln Laboratory, Lexington, MA

Rapidly adopting advanced commercial microelectronics into military systems is an effective approach to maintain competitiveness. However, as commercial products are not designed for DoD (Department of Defense) missions, it is critical to understand the risk of a military system relying on them. We have performed a security analysis on a multi-drone ISR (intelligence, surveillance, and reconnaissance) system using commercial MPSoCs (Multiprocessor-System-on-Chip). In this paper, we discuss our key findings which include security risks and practical mitigations.

28.3: SMART-I: Dual Core Trusted Execution Environment for Resource-Constrained Applications **(4:10)**

Eslam Y. Tawfik, Sherif A. Mohamed, Islam Elsadek, Sayed Elgendy, Ahmed Ghonem, Jeremy Porter, James D. Hardy, Waleed Khalil, Shane Smith, Xinmiao Zhang, Jingbo Zhou
The Ohio State University, Columbus, OH

Mark M. Tehranipoor, Fahim Rahman, Tanvir Rahman
University of Florida, Gainesville, FL

Hardware-assisted security provides a level of security that software cannot provide. A full range of hardware-assisted security methods are being advocated by the industry including trusted execution environment, crypto accelerators, random number generation and malware detection. Trusted Execution Environments (TEEs) are widely used to isolate security critical applications from the main application processor. Intel SGX, ARM TrustZone TEEs have been shown to be vulnerable to side-channel attacks due to poor isolation as they use virtual security processors inside the main application processor. Google's Titan TEE implements a dedicated security processor which has good isolation but very poor communication performance limiting its use cases. In this paper, we present STAMP, a TEE with an embedded FPGAs tightly attached to its system bus for better isolation, resources access management and side-channel immunity.

28.4: Fail-Safe Logic Design Strategies within Modern FPGA Architectures **(4:30)**

Jim Plusquellic
University of New Mexico, Albuquerque, NM

Andrew Suchanek, Tom Mannos
Sandia National Laboratories, Albuquerque, NM

Fail-safe computing refers to computing systems that revert to a non-operational safe state when a fault occurs. In this paper, we investigate circuit level techniques as mitigation strategies for implementing fail-safe computing processes on field- programmable gate arrays (FPGAs). We assess the propagation of fault effects through FPGA primitives, including lookup tables (LUTs), configurable logic blocks and switch boxes within the OpenFPGA architecture as a proxy for FPGAs in general. The analysis reveals additional vulnerabilities that exist within reconfigurable architectures compared to an equivalent application-specific integrated circuit (ASIC) that must be considered when designing redundant circuitry and checking logic. Using fault injection combined with simulation and formal methods, we compare an ASIC-proven fail-safe monitoring circuit, with data blocking and alarm capabilities, to the equivalent circuit implemented in OpenFPGA. We also explore FPGA-specific design strategies, such as fixing placement and routing to help constrain the possible fault propagation paths.

28.5: Antenna in Packaging (AiP), Security Assessment and Challenges for Assurance **(4:50)**

Liton Kumar Biswas, Aslam A. Khan, Yong-Kyu Yoon, Navid Asadizanjani
University of Florida, Gainesville, FL

A trend toward antenna in packaging is driven by the requirement for next-generation high-performance wireless communication applications. Integrating the antenna elements into the SiP provides a small form factor and therefore improves functionality. However, security may be compromised by the growing trend in semiconductors and their applications owing to the complexity and challenges of the electronics supply chain. This paper provides a detailed overview and unexplored supply chain vulnerability parameters for an antenna in packaging. From the security perspective, we aim to draw attention to the supply chain vulnerability threats of the antenna in packaging, followed by an assessment of AiP's security and reliability. This paper also discusses physical inspection techniques as a potential countermeasure, along with additional content as mentioned throughout the paper.

Wednesday Evening Social at San Diego Zoo **(7:30–9:30)**

Session 29

ADVANCED POWER ELECTRONICS

Wednesday, 22 March / 3:30 – 4:50 pm /
Town and Country Ballroom D

Chair: **Fritz Kub**
U.S. Naval Research Lab, Washington, DC

Co-Chair: **Travis Anderson**
U.S. Naval Research Lab, Washington, DC

29.1: **A History of Silicon Carbide (SiC) Wide Bandgap (WBG) Advancement through Power Electronic Building Blocks (PEBB) and Implications for the Future** **(3:30)**

Lynn "LJ" Petersen
Office of Naval Research, Arlington, VA

In 1994, the Power Electronic Building Block (PEBB) program was initiated by ONR. The PEBB program was an integrated program of material, device, circuit, and system science and technology (S&T) development The program's core objective was to reduce the size, weight, and cost (SWaP-C) of power electronics (PE) to realize PE shipboard power systems enabling future affordable and powerful electric warships. Since then much has been completed through PEBB advancement including revealing science and technology (S&T) gaps, (i.e., the need for soft magnetic materials to realize even higher power density PEBB systems.) The past half century has seen the advancement of material development of WBG technologies through the concerted efforts of ONR and the other DOD agencies, and have most recently harvested the fruit of the material advances of SiC into applications that will benefit both the DOD and industry. The future is bright for SiC WBG PEBB based technology.

29.2: **Power Devices and Systems for Gigawatt Grids in Flight: Electric Aviation** **(3:50)**

Isik Kizilyalli
U.S. Department of Energy Advanced Research Projects Agency – Energy, Washington, DC

Eric Carlson
Booz Allen Hamilton, Washington, DC

The electrical system on an all-electric aircraft needs to generate, regulate, and distribute power throughout the airplane and is analogous to the U.S. electric grid. An all-electric twin-aisle aircraft would need utility-scale power for takeoff making it a microgrid flying on the aircraft. Electrification of the aviation industry is the next big step in decarbonization reducing global greenhouse-gas emissions. The U.S. Department of Energy's Advanced Research Project Agency for Energy has invested over $100 million in an aviation electrification portfolio with significant efforts in key technology enablers including batteries, fuel cells, medium-voltage cables and connectors, circuit breakers, power electronic devices, electric motors, and motor drives. All the key technology efforts are focused on increasing the gravimetric power and energy density needed for the aviation industry. Development of these key technology enablers for aviation electrification will provide the U.S. a critical technological advantage in an increasingly electrified world economy.

29.3: T-Type Modular DC Circuit Breaker (4:10)

Baljit Singh Riar, Jeffrey Ewanchuk, Parag Kshirsagar
Raytheon Technologies Research Center, East Hartford, CT

Jin Wang
The Ohio State University, Columbus, OH

This paper presents a framework for the design of a T-type modular DC circuit breaker that can easily be scaled to a voltage rating of 20 kV. Experimental results of a 1 kV 500A T-breaker are presented in this paper to demonstrate feasibility of the concept. The breaker is over 99.5% efficient at 500A and is used to break a fault current of up to 4.24 kA. While the breaker is designed for commercial grid application through an ARPA-E funded program, it is broadly applicable for protection in naval power systems and other DoD applications and hence presented at this conference.

29.4: Beta-Gallium Oxide Junction Barrier Schottky Diodes with Sputtered P-Type Nickel Oxide (4:30)

Joseph Spencer, Alan Jacobs, James Gallagher, Karl Hobart, Travis Anderson, Marko Tadjer
U.S. Naval Research Laboratory, Washington, DC

Boyan Wang, Ming Xiao, Yuhao Zhang
Virginia Tech (CPES), Blacksburg, VA

Kohei Sasaki, Akito Kuramata
Novel Crystal Technology Inc., Sayama, Japan

29.5: WITHDRAWN

Wednesday Evening Social at San Diego Zoo (7:30–9:30)

Session 30

AI CONCEPTS & IMPLEMENTATIONS

Wednesday, 22 March / 3:30 – 5:10 pm / Palms Room 1-3

Chair: **Saverio Fazzari**
Booz Allen Hamilton, Clarksville, MD

Co-Chair: **Abirami Sivananthan**
InQTel, Arlington, VA

30.1: Hardware-based Acceleration of Explainable AI Models (3:30)

Zhixin Pan, Prabhat Mishra
University of Florida, Gainesville, FL

Machine learning (ML) is successful in achieving human-level performance in various fields. However, it lacks the ability to explain an outcome due to its black-box nature. While recent efforts on explainable ML has received significant attention, the existing solutions are not applicable in real-time systems since they usually lead to numerous iterations of time-consuming complex computations. In this paper, we propose an efficient framework to enable acceleration of explainable ML procedure with hardware accelerators. We explore the effectiveness of both Tensor Processing Unit (TPU) and Graphics Processing Unit (GPU) based architectures in accelerating explainable ML. Our proposed solution exploits the synergy between matrix convolution to take full advantage of TPU's inherent ability in accelerating matrix computations. This technology will enable real-time detection and localization of malicious implants (hardware Trojan) as well as malicious software (malware) attacks.

30.2: REX-SC: Range-Extended Stochastic Computing for Neural Network Acceleration (3:50)

Tianmu Li, Wojciech Romaszkan, Soumitra Pal, Sudhakar Pamarti, Puneet Gupta
University of California Los Angeles, Los Angeles, CA

Deep learning has grown in capability and size in recent years. Stochastic computing (SC) promises higher compute efficiency with its compact compute units, but accuracy issues have prevented wide adoption. In this work, we propose Range-Extended Stochastic Computing (REX-SC) to deal with the accuracy issues of stochastic computing. By modifying the functionality of OR-based SC accumulation, we increase computation accuracy without sacrificing the performance benefits. Our approach reduces the stream length needed for the same accuracy and improves the energy efficiency of SC. Our approach also improves training performance for SC-based neural networks and makes training SC models possible for large models.

30.3: Graph Neural Networks for Transfer of Performance Models Across Analog Circuit Topologies (4:10)

Zhengfeng Wu, Ioannis Savidis
Drexel University, Philadelphia, PA

Graph neural networks and transfer learning are leveraged to transfer device sizing knowledge learned from data of related analog circuit topologies to predict the performance of a new topology. The techniques are applied to transfer predictions of performance across four op-amp topologies in a 65 nm technology, with 10000 sets of sizing and performance evaluations sampled for each circuit. Results indicate that zero-shot learning with GNNs trained on data of three related topologies is effective for coarse estimates of the performance of the fourth circuit without requiring any data from the fourth circuit. Few-shot learning by fine-tuning the GNNs with a small dataset of 100 points from the target topology further boosts the model performance. The fine-tuned GNNs outperform the baseline artificial neural networks trained on the same 100 points from the target topology with an average reduction in the root-mean-square error of 70.6%. Applying the proposed techniques improves the sample efficiency of the performance models of the analog ICs.

30.4: Machine Learning at the Edge Using Neural Network Processors (4:30)

Edwin Lee
Raytheon Technology, Hanover, MD

Michael Parker
Raytheon Technology, El Segundo, CA

Machine learning, including deep learning, applications have gained traction in both the military and commercial sectors in recent years, enabling machine learning in tactical environments. This paper discusses the neural network processing architecture and why it surpasses all size, power, throughput, and weight requirements while maintaining performance and allowing interoperability with commercial vendors license comprehensive development environment and machine learning libraries as compared to machine learning models running on the CPU, GPU, and FPGA.

30.5: Efficient Dual-Mode Analog to Digital Converter for In-SRAM DNN Accelerators (4:50)

Shamma Nasrin, Amit Ranjan Trivedi
University of Illinois at Chicago, Chicago, IL

Wilfred Gomes
Intel, Hillsboro, OR

A memory structure performs most inference computations for compute-in-memory processing of deep neural networks (DNN). The analog processing of compute-in-memory creates significant challenges since ADC's necessity is directly linked with exploiting physics-based computations, i.e., utilizing charge or current-based representation of operands to sum them over a wire. Integrating an ADC with each compute-in-memory array aggravates challenges by reducing the on-chip silicon space for storing and operating on DNN parameters requiring more cycles to copy model weights from off-chip memories to on-chip structures. Thus, resulting in higher latency and energy for the processing. To improve the area efficiency of compute-in-memory arrays, we present a novel scheme of memory-immersed ADC in this work which utilizes the bit line capacitances of the compute-in-SRAM array for digitization. A 5-bit implementation of memory-immersed ADC achieves an average of ~10% area improvement. We introduce an efficient dual-mode digitization scheme enabling ~20% latency improvement.

Wednesday Evening Social at San Diego Zoo (7:30–9:30)

Panel Discussion

NDIA 3DHI WG

Wednesday, 22 March / 3:30 – 5:10 pm / Palms Room 4-6

This is a meeting of the 3D Heterogeneous Integration (3DHI) Working Group of the Emerging Technologies Subcommittee of the National Defense Industrial Association (NDIA) Electronics Division. This working group is focused on the immediate challenges in heterogeneous integration of die for defense microelectronics.

Wednesday Evening Social at San Diego Zoo (7:30–9:30)

THURSDAY, 23 MARCH

Continental Breakfast **(7:30–8:30)**

Session 31

RF TRANSMIT / RECEIVE MICROSYSTEMS

Thursday, 23 March / 8:20 – 10:00 am /
Town and Country Ballroom A

Chair: **Sanghoon Shin**
U.S. Naval Research Laboratory, Washington, DC

Co-Chair: **Adilson Cardoso PhD**
Raytheon Technologies, Roswell, GA

31.1: 0.1–18 GHz Ultra-Wideband Transceiver (8:20)

A. Kordovski, D. Galanos, E. Viveiros, A. Darwish, S. Hawasli
DEVCOM Army Research Laboratory, Adelphi, MD

Working under DARPA's Digital RF Battlespace Emulator (DRBE) program we designed, tested, and delivered an ultra-wideband Radio Frequency (RF) transceiver to interface with a Real-Time High-Performance Computing (RT-HPC) to create the world's first, large scale, virtual RF environment for developing, training, and testing advanced RF systems. The transceiver module works in conjunction with the RT-HPC and Xilinx's Zynq UltraSCALE+ family of processors to both generate and receive complex waveforms to create a high-fidelity and very low latency RF test environment. The first generation of the RF transceiver has a 0.1–18 GHz overall Bandwidth (BW) with a 1 GHz Instantons Bandwidth (IBW). The outputs of the transmitter and receiver signal paths are designed to accommodate a wide range of Systems Under Test (SUT), varying signal amplitudes, while also maintaining high Spur Free Dynamic Range (SFDR).

31.2: Wideband Integrated Digital Receiver for ELINT Bands Using Advanced Next-Generation Devices (8:40)

Kelly Cheung, Matthew Longbrake, Hunter Doster, Peter Buxa, Ouail Albairat, Kelly Darnell, Thomas Dalrymple
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

31.3: A Wideband 2 to 18 GHz Transmit-Receive Module **(9:00)**

Steve Nelson, Chris Ison, David Ignacio, Chris Turner, Rajah Vysyaraju, Mark Long, Dumitru Grecu
ENGIN-IC, Inc., Plano, TX

ENGIN-IC has developed an integrated Transmit -Receive (T/R) Front-End Module that offers significant performance improvements relative to the current standard. The module leverages ENGIN-IC's component technology to achieve the desired performance between 2 and 18 GHz in a size that fits the Ku-band grid spacing. The module incorporates GaAs, GaN, and Silicon technologies to realize the performance. For receive, the design incorporates three low noise gain stages to achieve near 30 dB gain and less than 4 dB noise figure including T/R switch losses. For transmit, the design offers 5 gain stages to achieve 2.5 W average Pout, 25 percent PAE with minus 5 dBm input including switch losses. A low loss T/R switch is used that has typical loss less than 1 dB maximum across the band. The module is built within a hermetic, Aluminum-Nitride (AlN) QFN package with dimensions of 11 mm × 6 mm × 1.5 mm.

31.4: SWaP Advancement of a Next Generation High Performance 0.5–55 GHz RF Front End **(9:20)**

Brad Hall, Benjamin Annino, Ahmet Balcioglu, David Yeh
Analog Devices, Inc., Wilmington, MA

This paper outlines a chipset being developed by Analog Devices Inc. that allows signal conditioning of frequency spectrum covering 0.5 to 55 GHz for use with next generation data converters. This chipset is designed to optimize size while maintaining a very high level of performance with the ability to quickly reconfigure based on the dynamic environment it is operating in. Included in this paper is an overview of the chipset architecture, descriptions of the overall SWaP (size, weight, and power) reductions, performance models and simulation results, as well as a discussion on a novel approach to addressing the stringent timing requirements for reconfigurability.

31.5: MIDAS Wideband mmW Digital Tile **(9:40)**

Lawrence J. Kushner, James McSpadden, Jason Milne, Richard Young, Enoch Arya
Raytheon Technologies, Dallas, TX

John D. Albrecht, John Papapolymerou, Matthew S. Hodek
Michigan State University, East Lansing, MI

Myung-Jun Choe, Jae-Yong Ihm, Kang-Jin Lee, Jonathan B. Hacker
Teledyne Scientific Co., Thousand Oaks, CA

BREAK **(10:00–10:30)**

Session 32

ADVANCED SENSORS

Thursday, 23 March / 8:20 – 9:40 am /
Town and Country Ballroom B

Chair: **Marcia Sawhney**
National Security Agency, Fort Meade, MD

Co-Chair: **Manuel Trejo**
DoD

32.1: VEViD: A Physics-Inspired Computationally Efficient Low-Light Enhancement Algorithm (8:20)

Callen MacPhee, Bahram Jalali
UCLA, Los Angeles, CA

This paper introduces a low light image enhancement algorithm that is derived directly from the physics of diffraction and coherent detection. The algorithm can enhance 4k video at over 200 frames per second which image quality comparable to the state-of-the-art deep learning algorithms but with 1–2 order of magnitude lower latency. The extreme computational efficiency makes it ideal for night vision enhancement on edge devices. We demonstrate how pre-processing visually-impaired images with VEViD improves the accuracy of object detection using off-the-shelf neural network algorithms without having to retrain them on low light conditions. Emulating physical processes, the algorithm has the potential to be direct implemented into optical hardware at the edge.

32.2: Verifying Floating-Point Digital Signal Processing Using Formal Methods (8:40)

Laureano Carrasco Costilla, Sean Safarpour, Ming Zhang, Jin Zhang
Synopsys, Inc., Mountain View, CA

Digital Signal Processing (DSP) processors perform high-speed numeric calculations used in both consumer electronics, industry instrumentation, as well as military and defense applications. Recent advancement in technologies, such as automated driver assistance systems (ADAS) and RADAR/LiDAR applications, have made floating-point DSP a requirement to support higher dynamic range and precision in data computation. Formal Methods have long been used to verify functional correctness of digital systems. Its exhaustive analysis based on mathematical proof can find corner case bugs and lead to full proof of design behaviors. Recent years, datapath validation using Formal Methods have gained adoption in many application spaces, because modern CPU, GPU, AI/ML, and DSP need to process large amount of data and perform complex computations.

32.3: Magnetoelectric Heterostructure for Passive Internet of Things Vibration Sensor Node Application **(9:00)**

Yifan He, Cunzheng Dong, Xiaxin Liu, Melania St. Cyr, Haoling Li, Nian-Xiang Sun
Northeastern University, Boston, MA

Vibration is an essential indicator of the performance of various mechanical machines, construction structure health condition, seismicity and motion/human activity. The vibration monitoring device is expected to be installed near the structures under monitoring and system integration as an internet of things (IOT) sensor node formed by vibration detection device, local power supply, and signal transmission device is necessary for further signal analysis and diagnosis. Here, we present the magnetoelectric (ME) heterostructure that composed of a piezoelectric material layer and highly magnetostrictive material layers with versatility working as a compact vibration detection sensor and energy harvesting device using stray magnetic field as energy source, with as-demonstrated capabilities of communication as a very low frequency (VLF) antenna, the ME heterostructure can potentially served as a great candidate for IOT vibration sensor node applications.

32.4: IRIS: Integrated Retinal Functionality in Image Sensors **(9:20)**

Akhilesh Jaiswal, Ajey Jacob
University of Southern California, Los Angeles, CA

Gregory Schwartz
Northwestern University, Chicago, IL

Maryam Parsa
George Mason University, Fairfax, VA

Neuromorphic image sensors draw inspiration from the biological retina to implement visual computations in electronic hardware. Gain control in phototransduction and temporal differentiation at the first retinal synapse inspired the first generation of neuromorphic sensors, but processing in downstream retinal circuits, much of which has been discovered in the past decade, has not been implemented in image sensor technology. We present a technology-circuit co-design solution that implements two motion computations occurring at the output of the retina that could have wide applications for vision based decision making in dynamic environments. Our simulations on Globalfoundries 22 nm technology node show that the proposed retina-inspired circuits can be fabricated on image sensing platforms in existing semiconductor foundries. Integrated Retinal Functionality in Image Sensors (IRIS) technology could drive advances in machine vision applications that demand robust, high-speed, energy-efficient and low-bandwidth real-time decision making.

BREAK **(10:00–10:30)**

Session 33

THE T&AM RAMP PROGRAM: RESULTS OF PHASE 2

Thursday, 23 March / 8:20 – 10:00 am /
Town and Country Ballroom C

Chair: **Linton Salmon**
DARPA, Arlington, VA

33.1: Rapid Assured Microelectronics Prototypes: Modernizing the Approach to Defense Microelectronics (8:20)

Cody Wagner
U.S. Naval Surface Warfare Center Crane Global Deterrence and Defense Department – Trusted Microelectronics Division, Crane, IN

The RAMP program addresses brand new technology development that will provide DoD relevant IC prototypes utilizing advanced node fabrication that mitigate the need for International Traffic in Arms Regulations (ITAR) fabrication. Rapid generation and assurance of microelectronic systems is directly relevant to enhancing the mission effectiveness of military personnel and the supported platforms, systems, and components acquired or developed by the DoD and enables assured microelectronics to be used by the services.

33.2: Enabling RAMP Through a Microsoft Azure Collaborative Design Platform (8:40)

Joseph Tostenrude, Prashant Varshney
Microsoft Strategic Missions & Technologies – Silicon, Irvine, CA

The DoD Rapid Assured Microelectronic Prototypes (RAMP) program provides secure, consistent, cloud-based capabilities and infrastructure for advanced semiconductor design and manufacture. The goal of RAMP Phase 2 is the establishment of a secure design capability that supports assured Defense Industrial Base (DIB) design in state-of-the-art (SOTA, defined as less than 22 nm) technology nodes. This secure design capability will apply repeatable methods to ensure confidentiality and integrity (C&I) of circuits during the design and fabrication flow, as well as the generation and collation of artifacts supporting DoD's Microelectronics Quantifiable Assurance (MQA) framework.

33.3: SiliconCompiler: A Cloud-Scale ASIC Build System with Support for Quantifiable Assurance (9:00)

Andreas Olofsson, Noah Moroze, William Ransohoff
Zero ASIC, Cambridge, MA

Hardware specialization for future SWAP constrained national security applications will require significant improvements in design efficiency and quantifiable assurance as compared to current defense industry best practices. In this work, we take a distributed approach to secure ASIC design, with the goal of creating infrastructure that scales to thousands of developers and millions of servers. Technical contributions in this work include (i) a standardized hardware build system manifest, (ii) a light-weight flowgraph based programming model, (iii) a client/server execution model, and (iv) a provenance tracking system for distributed development. In this work, we present an open source silicon build platform "SiliconCompiler" and references implementations for the Intel16 and GF12LP process nodes as part of the Integrated Design Framework (IDF) effort funded by the DoD Rapid Assured Microelectronics Prototypes (RAMP) program.

33.4: Intel and Quantifiable Assurance: Implementing MQA in a Commercial Foundry **(9:20)**

Joseph Yip, Ife Hsu
Intel Corporation, Hillsboro, OR

Intel is a major supplier for the Department of Defense (DoD), and in doing so has complied with the emerging Quantifiable Assurance specifications.

33.5: State-of-the-Art EDA in the Cloud: Rapid Assured Microelectronics Prototypes **(9:40)**

George Gerace, Robert Narumi, Monir Zaman
Raytheon Intelligence and Space, El Sugunda, CA

As the cost and complexity of modern military electronics systems continue to increase, dependance upon the advanced node (≤22 nm) semiconductors and highly integrated packaging required to enable them in also increasing. Meanwhile, the supply of advanced node semiconductor foundries is shrinking while the potential for malicious attacks on them is on the rise. Fundamentally, maintaining warfighter superiority requires a modern approach to advanced microelectronics design, supply chain security, and assured access to advanced node semiconductor manufacturing. RAMP (Rapid Assured Microelectronic Prototypes) is demonstrating the use of secure cloud microelectronics design capabilities, embedded hardware security, and the use of commercially available advanced node semiconductor fabrication capabilities to enable accelerated, secured, and assured development of modern electronic defense system.

BREAK **(10:00–10:30)**

Session 34

RADIATION HARDENED TECHNOLOGIES AND SYSTEMS

Thursday, 23 March / 8:20 – 9:40 am /
Town and Country Ballroom D

Chair: **Pauline Paki**
Defense Threat Reduction Agency, Fort Belvoir, VA

Co-Chair: **Tyler Lovelly**
Air Force Research Lab, Kirtland AFB, NM

34.1: **High-Productivity Direct Write E-beam Accelerates Early Concept Prototyping and High Mix Production of Trusted and Assured Microelectronics** **(8:20)**

K. MacWilliams, A. Ceballos, T. Prescop, R. Van Art, D. K. Lam
Multibeam Corporation, Santa Clara, CA

B. Ferguson, M. Nelson
SkyWater Technology, Bloomington, MN

Multibeam Corporation has built a Multicolumn Electron Beam Lithography (MEBL) system using its miniature column technology. The MEBL system has the flexibility to support a wide range of applications in Government microchip production. SkyWater Technology is preparing to integrate the MEBL system into its Bloomington facility to facilitate early concept prototyping and high-mix, low-volume production of advanced microchips to meet Government microelectronics needs.

34.2: **WITHDRAWN**

34.3: **A Radiation-Hardened Optical Transceiver in 180 nm CMOS Technology** **(8:40)**

Yu-Lun Luo, Chaerin Hong, Alexander Anderson, David Dolt, and Samuel Palermo
Texas A&M University, College Station, TX

Radiation in harsh operating environments can degrade the bit error rate (BER) of optical transceivers. This paper reports a radiation-hardened VCSEL-based optical transceiver operating at 0.5 Gb/s. By employing triple modular redundancy (TMR) and enclosed layout transistor (ELT) techniques, the BER = 10–12 sensitivity is anticipated to be improved. Both this radiation-hardened transceiver and a conventional non-radiation-hardened design will be tested at the Texas A&M Cyclotron Institute in November 2022. The optical transceiver's SEE sensitivity will be discussed in the final paper version.

34.4: A Technology Characterization Vehicle for Comprehensive Radiation Testing and Assurance in a 12/14 nm FinFET Process Node **(9:00)**

T. D. Haeffner, D. S. Vibbert, J. S. Kauppila, G. D. Poe, C. J. Moyers, W. T. Holman, L. W. Massengill
Reliable MicroSystems, LLC, Franklin, TN

Reported radiation test results by different research groups have varied widely for the same 12/14 nm FinFET process node, hampering the assessment of its radiation resiliency. To resolve observed discrepancies, we describe a comprehensive technology characterization vehicle (TCV) that incorporates an extensive matrix of transistor and logic device variants, thereby permitting a definitive radiation testing study and comparison of device choices in the technology. The design methodology underlying this TCV can be applied to additional integrated circuit processes.

34.5: GlobalFoundries Rad-Hard EcoSystem Vision **(9:20)**

Deniz Civay, Sebastian Ventrone, Ezra Hall
GlobalFoundries, Malta, NY

Stephanie Pusch
Trusted Semiconductors

Kristine Schroeder
Avalanche Technology, Fremont, CA

Dan Benveniste
NGC

Tom Wolf
Silicon Technologies

David Papini
BAE

John Damoulakis
Cadence

George Gerace, Helen Ying
Raytheon

Ian Land, Jeff Wetch
Synopsys

David Wallach, Ken Merkel
Nimbus Services

The radiation needs of the Aerospace & Defense (A&D) community within its platforms are diverse and unique compared with standard commercial models, creating complexities, challenges resulting in much longer design cycles. In recognition of some of these known challenges and a desire to accelerate the pace of innovation in this community with a vibrant A&D ecosystem, a broad working group has been created consisting of members from the Defense Industrial Base, IP suppliers, Fabless Semiconductor, GlobalFoundries, EDA and importantly with representation from additional government organizations. In its initial phase, the working group has created a set of visions in four primary topical areas identified early on by the group as being the highest priority. Expansion and evolution of these topical areas is likely over time. The first four topical areas (lanes) being driven, all with a backdrop of complexities resulting from radiation effects, currently include: Rad-Hard by Process, IP and Storefront, Data management, and Rad-Hard Design & EDA methodologies. This paper will summarize the collective vision of each of the working lanes and provide an overall collective summary. The intended result is improved understanding of a Radiation EcoSystem for the purpose of accelerating end platform development, improving efficiencies and throughput of the overall design process.

BREAK **(10:00–10:30)**

Session 35

ELECTRONIC MATERIALS RESEARCH

Thursday, 23 March / 8:20 – 10:00 am / Palms 1-3

Chair: **Craig Keast**
MIT Lincoln Laboratory, Lexington, MA

Co-Chair: **Daniel Radack**
Institute for Defense Analysis, Alexandria, VA

35.1: RF Performance of Diamond Transistors (8:20)

Dmitry Ruzmetov, James Weil, Leonard M. De La Cruz, Pankaj B. Shah, Mahesh R. Neupane, Derwin F. Washington, Stephen B. Kelley, Sergey Rudin, A. Glen Birdwell, Tony G. Ivanov
DEVCOM Army Research Laboratory, Adelphi, MD

Bradford B. Pate
U.S. Naval Research Laboratory, Washington, DC

Diamond is an ultra-wide bandgap semiconductor with unique properties. It has the highest thermal conductivity of all materials. Also, it has a bandgap of 5.47 eV, critical electric field of 13 MV/cm, and demonstrated carrier concentration in two dimensional hole gas of ~10^{14} cm^{-3}. Therefore, diamond is being considered as the next generation semiconductor for RF applications. We present results for diamond RF MOSFETs where the channel conductivity is enabled by diamond hydrogenation and Al_2O_3 acceptor layer. The diamond wafer shows the sheet resistance of 5.6 kOhm/sq after the device fabrication. The MOSFETs achieve the drain current of Id = 408 mA/mm (Vgs = –3 V) and the transconductance g_m = 120 mS/mm (Vgs = –1 V) at Vds = –10 V. The devices demonstrate break-down voltage of 134 V on 1.7 µm SD spacing (0.8 MV/cm on average). The small signal short circuit current cutoff frequency is f_t = 20 GHz and power gain cutoff frequency f_{max} = 39 GHz for Lg = 200 nm FETs. The largest output power density at 4 GHz is 0.92 W/mm. Work is under way to reduce the high frequency current compression and push this technology further towards the high RF power applications.

35.2: Polarization-induced Two-dimensional Electron-gas (2DEG) and Hole-gas (2DHG) in Grafted AlN/GaN Heterostructures (8:40)

Seunghwan Min, Ranveer Singh, Jiarui Gong, Haris Naeem Abbasi, Jie Zhou, Daniel Vincent, Moheb Sheikhi, Neil Campbell, Jingcheng Zhu, Yang Liu, Mark Rzchowski, Zhenqiang Ma
University of Wisconsin-Madison, Madison, WI

Ping Wang, Ding Wang, Zetian Mi
University of Michigan, Ann Arbor, MI

Timothy Grotjohn
Michigan State University, East Lansing, MI

We have investigated the two-dimensional hole gas (2DHG) phenomenon at the interface of grafted single-crystalline N-polar AlN and Ga-polar GaN heterostructure. An ultrathin layer of oxide was used at the interface of AlN/GaN to effectively passivate the surface defects and to improve the bonding between them at the needed temperature for the grafting process. Using careful design for epitaxial growth of AlN and device fabrication, the AlN/GaN heterostructure exhibits the carrier density and Hall mobility of 3.63 × 10^{12} cm^{-2} and 36.1 $cm^2V^{-1}s^{-1}$, respectively owing to the formation of 2DHG channel. The outstanding performance of the AlN/GaN device offers a possibility for the application of 2DHG-based high frequency PFET devices.

35.3: Gallium Nitride Deposited on SiO_2 by RF-Biased Atomic Layer Annealing at 275 °C (9:00)

Aaron J. McLeod, Andrew Kummel, Ping Che Lee, Scott Ueda
University of California, San Diego, La Jolla, CA

This report demonstrates atomic layer annealing (ALA) for depositing GaN thin films with columnar morphology on SiO_2 at 275 °C. Following each precursor dosing cycle, a short argon or krypton plasma treatment step with substrate bias was used to crystallize the film. Tuning the incident ion momentum by adjusting the substrate bias was studied and is crucial to healing defects on and below the growth surface through collision cascades without exceeding sputtering and implantation thresholds. The results demonstrate that RF-biased ALA outperforms nonbiased ALA process and thermal ALD, and that ALA is a viable technique for oxygen-sensitive micro-LED fabrication at low temperature.

35.4: Ultracompact and Conformal Magnetodielectric Antennas for HF and VHF (9:20)

Yifan He, Nian X. Sun
Northeastern University, Boston, MA

James Cheng, P. Venkat Parimi, Xiaoling Shi, Hwaider Lin
Winchester Technologies, LLC, Burlington, MA

Mohan Sanghadasa
US Army DEVCOM Aviation & Missile Center, Redstone Arsenal, AL

Novel approaches are needed to improve the performance and reduce the size, profile, number, and signature of antennas with significantly enhanced efficiency in HF-UHF. It has been recently shown that hesitivity is directly linked to the radiation efficiency of magnetodielectric antennas, which is the maximum magnetic conductivity, can characterize the performance of magnetic materials and categorize the radiation efficiency of magnetodielectric antennas; the higher the hesitivity, the higher the attainable efficiency in these magnetodielectric antennas. Here, we demonstrated new ultracompact conformal VHF magnetodielectric antennas based on commercially available ferrite ceramic substrates. These VHF magnetodielectric antennas show enhanced gain and bandwidth, ground plane immunity, and significantly reduced antenna size by ~10× compared to monopole antennas. State-ofthe-art hesitivity as high as 6×10^6 Ω/m has been reported in CoZrNb alloy films. Further hesitivity improvement by 10× over state-of-the-art is expected for magnetic films on a thin carrier substrate. We expect that new magnetic materials with higher hesitivity will be demonstrated, which will lead to new magnetodielectric antennas with further enhanced radiation efficiency and ground plane immunity.

35.5: MBE Growth of GaSb/InAs Type-II Superlattice Structures (9:40)

Iqbal Ali, Wey Lee, Brad Lenzen, Rafiqul Islam
Cactus Materials, Inc., Tempe, AZ

The use of GaSb/InAs type-II superlattice structures grown on GaAs or GaSb substrates provide an interesting pathway to achieve detectors that can operate in multiple regimes based on the thickness of individual layers in the superlattice and number of periods in the structure. This work focuses on the MBE growth of GaSb and InAs on GaSb and GaAs substrates to create a baseline for the Type-II superlattice structure (T2SL) structures. The grown layers are characterized using HR-XRD and PL to understand the structural and optical properties. Finally, a growth template to get high quality T2SL structures on both GaSb and GaAs are discussed. In addition, a TCAD based simulation will be used to estimate the material properties of the grown epilayers.

BREAK (10:00–10:30)

POSTER SESSION

Thursday, 23 March / 10:30 am – 12:10 pm /
Golden State Ballroom

P.1: Radiation Effects Testing Capabilities with Heavy-Ions at Michigan State University

Steve Lidia, Guillaume Machicoane, Doug McNanney, Peter Ostroumov, Andreas Stolz, Abe Yeck
Michigan State University, East Lansing, MI

Michigan State University has recently commissioned and begun operations of a new radiation effects beamline designed for single event effects testing with heavy ions. We present the capabilities of the beamline and control areas to support user operation and device testing. We report measurements of beam purity, beam energy and beam distribution, and instrumentation to monitor and report real time dosimetry. Finally, we discuss facility development plans to support both immediate user needs and the longer-term needs of the radiation effects testing community.

*MSU designed, established, and operates FRIB as a DOE Office of Science National User Facility in support of the mission of the Office of Nuclear Physics under Cooperative Agreement DE-SC0000661.

P.2: Total Ionizing Dose Response of a Novel Precision Oscillator Implementation

Giovanni Esteves, Todd M. Bauer, Michael P. King
Sandia National Laboratories, Albuquerque, NM

With this work we report on total ionizing dose response of an integrated oscillator that uses an aluminum nitride-based microelectromechanical (MEMS) resonator as the frequency source with a silicon CMOS integrated circuit controlling the resonator. For this instantiation the resonator and integrated circuit are assembled on a printed circuit board, however, the components are amenable to a future system-in-package integration. The integrated system was exposed to X-rays from an ARACOR 4100 X-ray irradiator, with total dose ranging from 0 to 200 krad (SiO_2). Over the total range of dose, we measured an increase in frequency from 38.794 MHz to 38.799 MHz, or about 120 ppm. Phase noise remained constant at 400fs. Total system current increased from 63.09 mA to 63.28 mA. We discuss some of the complexities associated with characterizing total dose response of an integrated system.

P.3: High-Density, High-Endurance and High-Reliability STT-MRAM Enabling Next Gen Space Systems

Paul Chopelas, Kristine Schroeder
Avalanche Technology, Fremont, CA

The advancement and optimization of satellite architectures has been in part hindered by limitations of suitable memory technologies. This paper will illuminate why increasing processing requirements of next gen systems in avionics and space require high density, performance, endurance, reliability, and low power memories to maximize potential innovation and what options exist to support this. Specifically, one such example, Avalanche Technology's third generation Spin Transfer Torque Magnetoresistive Random Access Memory (STT-MRAM) technology redefines advanced memory utilization for a variety of applications including those within Aerospace & Defense (A&D).

P.4: A New Design and Fabrication of Radiation Hardened Low Gain Avalanche Detector

Iqbal Ali, Wey Lee, Brad Lenzen, Rafiqul Islam
Cactus Materials, Inc., Tempe, AZ

We demonstrated a new design and fabricated a radiation hardened low gain avalanche detectors for fast timing and space resolutions. This detector was based on an engineering substrate which were characterized and validated by building a full diode structure resulting in low leakage current, showing no degradation when the depletion region reaches the interface between the two wafers. TCAD simulation confirmed its effectiveness to develop radiation hardened high fill factor LGADs. What is most exciting the uniqueness of the engineering substrate fabrication which can be applicable to introduce "radiation hardness" properties into other types of sensors development such as hybrid, pixel sensors, CMOS, and CCD sensors.

P.5: A Comparison of 25 GHz-LC-VCO Circuit Topologies for SEU Mitigation in 22 nm FinFET

David Dolt, Inhyun Kim, Yu-Lun Luo, Samuel Palermo
Texas A&M University, College Station, TX

Three LC-tank voltage-controlled oscillators (VCOs) are designed in a 22 nm FinFET process with varactor and tail filter permutations to compare their sensitivity to single event effects (SEEs) and understand the overhead these circuit techniques have on the electrical performance. Each VCO has a tuning range from 15.8–25.9 GHz yielding a tuning aware FOM of 190.53 dBc/Hz. Furthermore, these VCOs where tested at the Texas A&M Cyclotron Institute at LET levels of 10, 35, and 70 MeV.cm^2/mg. These results showed both a marked decrease in cross sectional area when using the rad hard varactor tank configuration and the effectiveness of the LC tail filter for both phase noise and SEE mitigation.

P.6: An Automated Method for Adding Resiliency to Aerospace and Defense SoC Designs

Mary Ann White
Synopsys, Inc., Sunnyvale, CA

Adding safety measures to system-on-chip (SoC) designs in the form of radiation-hardened elements or redundancy is essential in making Aerospace and Defense (A&D) applications more resilient against random hardware failures that occur. Designing for safety does impact semiconductor development where these safety measures have generally been inserted manually by designers. Manual approaches can often lead to errors that cannot be accounted for. Synopsys has created a fully automated implementation flow to insert various types of safety mechanisms which can result in more robust and reliable SoC designs for A&D applications.

P.7: Automated Framework for Enhancing Existing Designs for Radiation-Tolerance

Georgios D. Dimou, Moises Herrera, Cole Sherrill, Tynan McAuley
Niobium Microsystems, Inc., Dayton, OH

Peter A. Beerel
University of Southern California, Los Angeles, CA

The reliability of integrated circuits subject to ionizing radiation is a concern for aerospace and defense applications. A recently proposed technique called Soft Error Resilient Asynchronous Design (SERAD) that addresses the dominant class of errors caused by radiation phenomena, called Single-Event Effects (SEE), promises state-of-the-art performance, energy, radiation tolerance and optimized error-recovery time using predominantly unhardened standard library cells. In this work we present a novel design flow that converts any of Niobium's non-hardened digital designs into SERAD hardened designs. The framework uses a Hardware Construct Language (HCL) for the design description and a small custom standard cell library to augment existing commercial libraries. The main benefits are twofold: (a) Easy deployment of SERAD to yield circuits that are both radia-

tion-tolerant and closer to the unhardened counterpart in terms of power, performance and area (PPA). (b) Fast prototyping and design turnaround, for improved development and reduced engineering cost.

P.8: Security Validation of Trusted Execution Environments

Hasini Witharana, Prabhat Mishra
University of Florida, Gainesville, FL

Trusted Execution Environment (TEE) relies on isolation properties in hardware architecture to ensure that client code and data in applications, containers or virtual machines can neither be deciphered (confidentiality) or modified (integrity) by untrusted parts of the system software stack such as a hypervisor provided by the cloud vendor. There are two fundamental challenges in TEE security verification: (i) how to derive security properties since security guarantees involve complex interactions between TEE hardware, firmware, and software stack, and (ii) how to verify such complex properties to prove that any hardware security assurances that the software relies on can be trusted. In this paper, we develop a comprehensive and scalable framework for TEE security verification using property checking.

P.9: Brain-Inspired Neural Adaptation for Dynamic and Scalable Hyperdimensional Learning

Zhuowen Zou, Mohsen Imani
University of California Irvine, Irvine, CA

Farhad Imani
University of Connecticut, Mansfield, CT

Haleh Alimohamadi
University of California Los Angeles, Los Angeles, CA

Rosario Cammarota
Intel Labs, San Diego, CA

In the Internet of Things (IoT) domain, many applications are running machine learning algorithms to assimilate the data collected in the swarm of devices. Sending all data to the powerful computing environment, e.g., cloud, poses significant efficiency and scalability issues. A promising way is to distribute the learning tasks onto the IoT hierarchy, often referred to edge computing; however, the existing sophisticated algorithms such as deep learning are often overcomplex to run on less-powerful and unreliable embedded IoT devices. Hyperdimensional Computing (HDC) is a brain-inspired learning approach for efficient and robust learning on today's embedded devices. Encoding, or transforming the input data into high-dimensional representation, is the key first step of HDC before performing a learning task. All existing HDC approaches use a static encoder; thus, they still require very high dimensionality, resulting in significant efficiency loss for the edge devices with limited resources. In this paper, we have developed NeuralHD, a new HDC approach with a dynamic encoder for adaptive learning. Inspired by human neural regeneration study in neuroscience, NeuralHD identifies insignificant dimensions and regenerates those dimensions to enhance the learning capability and robustness. We also present a scalable learning framework to distribute NeuralHD computation over edge devices in IoT systems. Our solution enables edge devices capable of real-time learning from both labeled and unlabeled data. Our evaluation on a wide range of practical classification tasks shows that NeuralHD provides 5.7× and 6.1× (12.3× and 14.1×) faster and more energy-efficient training compared to the HD-based algorithms (DNNs) running on the same platform. NeuralHD also provides 4.2× and 11.6× higher robustness to noise in the unreliable network and hardware of IoT environments as compared to DNNs.

P.10: Radiation Effects on Cybersecurity of Space Systems with COTS Processors

Benjamin Nahill, Ben Heberlein, Jeffrey Hughes, Donato Kava, Alice Lee, Jeffery Lim, Aaron Mills, Eric Simpson, Michael Vai, Roger Khazan
MIT Lincoln Laboratory, Lexington, MA

Keith Bergevin, Pawan Gogna
Defense Microelectronics Activity (DMEA), McClellan, CA

P.11: Cost Function Assisted Fuzz and Penetration Testing for SoC Security Verification

Hasan Al Shaikh, Muhammad Monir Hossain, Kimia Zamiri Azar, Fahim Rahman, Farimah Farahmandi
University of Florida, Gainesville, FL

Security verification of System-on-Chips (SoCs) has become a challenging endeavor due to the increasing complexity of design, the prevalence of security unaware design practices, and the introduction of numerous untrusted entities through a globalized supply chain. Existing verification methodologies and EDA tools utilized in contemporary practice suffer from scalability, the inability to capture detailed HW interactions, and the need for expert knowledge on the design and manual efforts. To overcome the current challenges, we propose an automatic, scalable, gray-box model, and a cost-function guided SoC security verification framework which is implemented in two approaches, fuzz and penetration testing (already proven as state-of-the-art in software security). Our experiments on an open-source RISCV-based SoC show the efficiency of the framework for both fuzz and penetration testing for generating edge-case inputs to trigger the vulnerability conditions with faster convergence.

P.12: Defending Elliptic Curve Cryptography against Laser Fault Injection Attacks

Khushboo Rani, Emma Andrews, Aruna Jayasena, Prabhat Mishra
University of Florida, Gainesville, FL

P.13: A Novel IoT Device Authentication Scheme Using Zero-Knowledge Proofs

Joshua Hovanes, Yadi Zhong, Ujjwal Guin
Auburn University, Auburn, AL

Due to growth of IoT devices across diverse applications, it has become essential to secure edge devices against hardware attacks such as tampering and cloning. A tampered device can bypass security measures implemented in software. One way to verify the authenticity of a device is by using physically unclonable functions (PUFs) as a unique fingerprint. During authentication, the PUF response from the edge device is transferred securely and compared with the stored response. This requires a secure communication between the edge device and server, and storage of the device fingerprint. In this paper, we propose a protocol using zero-knowledge proofs (ZKPs) that allows the prover to provide evidence of the fingerprint without revealing it. The edge device, the prover, convinces the server, the verifier, of a valid PUF response without storing it on the server. We propose using zk-SNARK, a popular ZKP protocol, for constructing the PUF authentication framework.

P.14: WITHDRAWN

P.15: Formal Equivalence Checking for Locked and Redacted Hardware Designs

Maneesh Merugu, Md Moshiur Rahman, Aritra Dasgupta, Swarup Bhunia, Sandip Ray
University of Florida, Gainesville, FL

Nij Dorairaj, David Kehlet, Kostas Amberiadis
Intel Corporation, Santa Clara, CA

Hardware obfuscation is an established technique for protecting hardware intellectual properties from supply-chain attacks. However, errors in implementation of obfuscation algorithms can undermine the protection provided. In this paper we design a compositional sequential equivalence checking technique to establish correctness of obfuscated designs. Our approach is agnostic to the underlying obfuscation technology and can be applied to both augmentation-based and redaction-based obfuscations. Our experimental results show that the SEC framework can easily scale to large designs, e.g., it can discharge equivalence verification of designs with 10s of thousands of gates in a few seconds.

P.16: An ISA-based Software Snippet Generation for Exploiting Hardware Vulnerabilities

Sree Ranjani Rajendran, Shams Tarek, Hadi M. Kamali, Farimah Farahmandi
University of Florida, Gainesville, FL

Systems-on-chip (SoCs) have become increasingly large and complex, resulting in new threats and vulnerabilities, mainly related to system-level flaws. However, the system-level the verification process, whose violation may lead to exploiting a hardware vulnerability is not studied comprehensively due to the lack of decisive (security) requirements and properties from the SoC designer's perspective. To enable a more comprehensive verification for system-level properties, this paper presents HUnTer (Hardware Underneath Trigger), a framework for identifying sets (sequences) of instructions at the processor unit (PU) that unveils the underneath hardware vulnerabilities. The HUnTer framework automates (i) threat modeling, (ii) threat- based formal verification, (iii) generation of counterexamples, and (iv) generation of snippet code for exploiting the vulnerability. The HUnTer framework also defines a security coverage metric (HUnT Coverage) to measure the performance and efficacy of the proposed approach. Using the HUnTer framework on a RISC-V-based open-source SoC architecture, we conduct a wide variety of case studies of Trust-HUB vulnerabilities to demonstrate the high effectiveness of the proposed framework.

P.17: Quantitative Assessment of Two-Photon Optical Beam Induced Current for Microelectronics Verification and Validation

Ryan J. Patton, Anthony George, Adam Kimura
Battelle Memorial Institute, Columbus, OH

Jamin McCue
Air Force Research Laboratory, Dayton, OH

P.18: Printed Circuit Board Design Verification Using X-ray Computed Tomography and Laminography

John True, Navid Asadi
University of Florida, Gainesville, FL

Chris Peitsch
Avonix Imaging, Maple Grove, MN

X-ray Computed Tomography (CT) is used non-destructively to extract design or manufacturing information from a product or sample. In the case of a printed circuit board (PCB), this physical inspection is often used to verify the device's design and functionality of its connected circuitry. As the complexity of PCB designs have become more sophisticated, there is a constant need for more capable physical inspection tools each year. X-ray inspection has been demonstrated as an effective tool for non-destructive

analysis, however, the noise and artifacts of complex PCB designs can inhibit automated inspection. The combination of X-ray Computed Tomography (CT) with Computed Laminography (CL) offers the benefits of a large field of view (CT) and high spatial resolution (CL) to provide hardware assurance for complex PCB designs.

P.19: Foundational Elements for Composable Security

Christopher Taylor, Rebekah Cross, Jacob Fallica, Jeremy Bellay
Battelle Memorial Institute, Columbus, OH

The role that hardware plays in cyber security has been increasingly recognized in recent years, especially as a source of security vulnerabilities and supply chain uncertainty. However, it has been difficult to evaluate the realism of theorized security attacks in the lifecycle of microelectronics from design to disposal. Similarly, the real risk transferred from hardware components to larger systems has been difficult to estimate and compare with other more conventional cyber security issues. Here, we discuss the foundation of creating composable system security models that can span the silos of the microelectronics lifecycle, as well as the levels of abstraction between component integration and platform assurance.

P.20: BAT: Boolean Algebraic Transformation on eASIC

Zhaokun Han, Aneesh Dixit, Satwik Patnaik, Jeyavijayan Rajendran
Texas A&M University, College Station, TX

Kostas Amberiadis
Intel Corporation, Santa Clara, CA

Structured application-specific integrated circuit (ASIC), a.k.a eASIC, is an intermediary technology between ASIC and field-programmable gate array (FPGA). On the eASIC platform, partial functionality is configurable and programmable, and the implemented design can achieve lower power, performance, and area costs than the same design on an FPGA. Moreover, eASIC has a shorter design cycle of around 2 months compared to the design cycle of the traditional ASIC (18 months). Similar to ASIC and FPGA platforms, the eASIC platform faces security threats, such as intellectual property (IP) piracy and reverse engineering. Thus, it is imperative to protect eASICs against the aforementioned threats. Logic locking is a countermeasure protecting design IP against these threats. This work discusses a logic locking technique, Boolean Algebraic Transformation (BAT), that protects the design IP implemented on eASIC. BAT offers two solutions on eASIC, satisfying different design constraints and enabling flexibility for designers without compromising security.

P.21: IOLock: An Input/Output Protection Scheme for Chip and PCB Protection

Christopher Vega, Patanjali SLPSK, Swarup Bhunia
University of Florida, Gainesville, FL

Reverse-Engineering poses a significant threat to the modern distributed electronic supply-chain. While there exist techniques like Logic locking at the chip-level and camouflaging at the board-level to combat reverse-engineering, the advent of SAT-based, and 3D Imaging attacks have shown that these protections can be bypassed. We observe that a common unifying factor that contributes to the success of these attacks is the ability of the attacker to observe the input/output (I/O) patterns. The attacker leverages this information by comparing with the I/O behavior of an unlocked circuit. We leverage this observation and present a novel locking scheme for called IOLock. IOLock restricts access to the actual inputs/outputs of the chips in a PCB by encoding/decoding modules near the I/O ports. The encoding/decoding modules are designed using to work with the existing JTAG infrastructure. IOLock aims at preventing chip and board-level reverse engineering attacks by locking the I/O ports.

P.22: Scalable Semi-formal SoC Security Validation

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This paper presents a semi-formal System-on-Chip (SoC) security verification technique, targeting Register Transfer Level (RTL) security vulnerability detection. It extracts critical process flows from a RTL design and executes RTL-level concolic testing to generate security test cases for identifying critical exploits manifested in a SoC. Furthermore, this technique can be adapted with for security validation of Commercial off-the-shelf (COTS) ICs, which are integral components of many modern SoCs. While avoiding combinatorial explosion, our experimental results demonstrate that in circumstances where conventional security verification tools are limited, the proposed technique furnishes significantly improved efficiency in detecting security vulnerabilities.

P.23: Design Data Security in Manufacturing Data Flows

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After a VLSI design is completed and a file representing the physical design is delivered to a foundry for fabrication, substantial data processing such as Optical Proximity Correction (OPC) is performed. The transmission, storage, and transformation of the design data during manufacturing opens up several points of attack for a malicious actor to degrade or alter the design. Potential consequences could include unintended functionality, reduced yield, or reduced performance. This paper provides a description of the data flow from an initial physical design through the photomask fabrication process. It identifies attack points where a malicious actor could damage the integrity of the design. It then evaluates strategies to mitigate risks of successful attacks, as well as improving traceability to identify the point sources of attacks.

P.24: Root Causing and Automatic Patching of Fault Injection Vulnerabilities

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Fault Injection (FI) attacks are versatile attacks that compromise the security of physical devices. Post-silicon testing allows identifying FI vulnerabilities, establishing the effectiveness and impact of FI on the security of the device. However, it is often unclear what part of the hardware/software was actually faulted and thereby identifying the root cause of the vulnerability. Consequently, implementing mitigations is a manual and exhaustive process. We propose a flexible framework that allows root causing FI vulnerabilities by simulating FI attacks, enabling both manual and automatic mitigations. These simulations can target hardware/software running on various CPU architectures. Our framework can simulate effects of single/multiple bit flips in any wire/logic gate by exhaustive enumeration strategies. We present a case study that root causes a PC hijack vulnerability on a RISC-V core and additionally show we can automatically harden the netlist against single-bit PC hijack faults with only 0.8% overhead.

P.25: New DBF ASIC for System SWaP-C Improvements and Root of Security IP for Hardware Security in Next Generation Digital AESAs

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Northrop Grumman Corporation, Linthicum, MD

Thomas Dalrymple, Peter Buxa, Matthew Longbrake
Air Force Research Laboratory, Wright-Patterson AFB, OH

P.26: Silicon Lifecycle Management Infrastructure Pivots to Detect Security Breaches

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The potential to use embedded sensors and supporting infrastructure to detect hardware security attacks is a good use of existing device- and system-level information sources embedded in an SoC (system on chip). These integrated circuit package-level sensors and monitors have been available for some time, but their application emphasis has usually been on performance, reliability, and safety. By coupling existing and novel sensor technology with in-system and cloud-based analytics, it is possible to detect and mitigate the efforts of hardware hackers as they try to apply their skills to uncover the secrets and capabilities stored inside today's advanced electronics. This paper will review sensors and supporting infrastructure and their capabilities to help detect and mitigate a security breach.

P.27: Efficient Activation of Stealthy Triggers in Hardware Trojans

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Hardware Trojans (HT) are one of the major concerns due to supply chain vulnerability. It can get introduced during different stages in the design cycle. Existing test generation-based HT detection techniques have several practical limitations. These approaches are designed to activate rare signals while ignoring rare transitions. Moreover, these approaches are not scalable for industrial designs. In this paper, we propose a scalable test generation framework to address the above challenges. Our threat model assumes that an adversary may exploit rare events consisting of rare signals (states) as well as rare branches (transitions). We propose a scalable framework for detecting hardware Trojans using Automated Test Pattern Generation (ATPG) based activation of rare events. Specifically, we utilize the complementary abilities of N-detection and maximal clique activation of rare events to generate efficient test patterns. Experimental results demonstrate that our ATPG-based framework significantly outperforms the state-of-the-art test generation-based HT detection techniques.

P.28: Memometer: Passive and Active Memory PUF-Based Hardware Metering Methodology for FPGA Supply Chain Security

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FPGAs offer faster prototyping and reduced time-to-market when compared to ASIC based systems. As the microelectronic industry has shifted to a horizontal ("fabless") model, FPGA counterfeiting, cloning, and over building has become a significant semiconductor supply chain issue. Identification and authentication of FPGA ICs are a tremendous challenge to government (DoD) and commercial entities. In this paper we present Memometer, a supply chain security tool that is used to 1) generate unique unclonable fingerprints based on a novel memory PUF design using FPGA look-up tables (LUTs) and 2) use these fingerprints to identify and authenticate ICs. Our methodology can generate millions of fingerprints per FPGA. We present temperature test results to characterize Memometer performance between –15 °C to 70 °C. It should be noted that we have also added error correction to compensate for both environmental and aging conditions, and we are improving our PUF design to make it a stronger.

P.29: Preserving Confidentiality and Anonymity in NoC-based SoCs

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Network-on-Chip (NoC) has become the backbone of communication between Intellectual Property (IP) cores in a System-on-Chip (SoC). We present a lightweight encryption and anonymous routing protocol for communication between IP cores in NoC-based SoCs. Our method eliminates the major overhead associated with traditional encryption and anonymous routing protocols using a novel lightweight protocol while ensuring that the desired security goals are met. Experimental results demonstrate that existing security solutions on NoC can introduce significant (1.5×) performance degradation, whereas our approach provides the same security features with a minor (4%) impact on performance.

P.30: Physically Secure Hardware Redaction and Logic Locking with Hybrid Logic Systems

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While hardware obfuscation techniques like logic locking and hardware redaction can secure chips against algorithmic attacks, security against physical attacks requires the use of emerging technologies with large error rates. Hybrid logic systems have therefore been proposed in which polymorphic islands with physical security provide algorithmic security within a large CMOS system. In this work, we demonstrate that a well-chosen encryption of small, physically secure islands embedded in a physically insecure technology is sufficient to secure the entire chip against algorithmic and physical attacks.

P.31: Embedded FPGA Assurance Lessons Learned: Independent Assessment and Bitstream Verification on a Commercial eFPGA

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Embedded FPGAs can add flexibility and security to government systems that rely on custom advanced microelectronics. The ability to control all aspects of programming and provisioning while incorporating the right mix of processing and sensing capabilities makes these a compelling alternative to traditional, one-size-fits-all, FPGAs. The necessity of having access to the files required to produce the eFPGA macro in the target technology also provides a unique opportunity to independently evaluate the IP for trusted and secure operation. In this report, we describe the platform and design assurance techniques developed for a commercial eFPGA. In this, we first perform a top-down and bottom-up analysis of the eFPGA tile as a whole and the configuration infrastructure in particular. We then lay down the framework for performing an independent functional and timing analysis of each programmed bitstream with full visibility of the fabric upon which it operates.

P.32: A Hardware/Software Architecture for System-on-Chip Security

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An architecture of a secure system-on-chip is presented in this paper, along with validation and the low overhead in performance and resource. The architecture extends the FLASK paradigm to hardware to ensure that threads isolated in software remain isolated when accessing hardware IP on the same device. The case study shows that the security components can successfully mitigate the attack scenarios and the overhead results show that the area and power overhead is minimal.

P.33: AFIx: An Automated Tool for Fault Injection Attack Assessment and Protection

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Several contemporary fault injection (FI) attack methods have been shown to be more effective at smaller process sizes. As this current trend continues and FI methods become more sophisticated, the need to develop an automated industry solution to the threats of FI increases. The Assessment of Fault Injection Extension (AFIx) aims to fill this need by providing the ability to both assess FI vulnerability and apply low overhead countermeasures at the gate level. AFIx achieves this using multiple novel methods, such as the application of FI models for generating potential fault lists and the use of time-to-digital (TDC) sensors for localized FI detection and access control.

P.34: Low-overhead Hardware Redaction Using Bitstream Compaction

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Nij Dorairaj, David Kehlet
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Hardware redaction has emerged as a promising countermeasure to thwart confidentiality and integrity attacks by untrusted entities in the globally distributed supply chain. However, the redaction techniques proposed in recent literature also incur high overhead costs, which makes them less suitable for real-world design requirements. We propose RIPPER 2.0, a fine-grained redaction methodology that employs novel optimization techniques to reduce overheads without compromising security. RIPPER 2.0 combines security-aware bitstream compaction with custom standard-cell-based programmable fabric to reduce overheads. We also evaluate the overhead reduction in RIPPER 2.0 on open-source benchmarks.

P.35: Improving Image Preprocessing for Counterfeit Microelectronic Detection

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Microelectronic counterfeiting and countermeasures are a multi-billion dollar industry which continues to grow. This large flow of goods, combined with globalized supply chains, means significant quantities of electronic goods must be inspected when arriving onshore by entities like DHS personnel. Since manual review of each sample is cost-prohibitive, error-prone and unscalable, advanced techniques including automated optical inspection (AOI) must be employed and improved to meet growing market demands. While machine learning (ML) techniques are growing in popularity to address this need, there is a lack of corresponding datasets to allow them to generalize across unknown samples for defect and counterfeit analysis. Toward this end, we propose several ways in which simple image preprocessing techniques can be used to greatly improve a generative neural network's ability to learn meaningful information about component characteristics. Through experimentation, we show how such approaches differ from standard ML pipelines and the specific benefits they provide.

P.36: Enabling Trust and Assurance for Third-Party IP by Generating Verifiable Security Evidence

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P.37: Robust Verification Architecture for Physical Inspection-based Chiplet Authentication

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Heterogenous Integration (HI) of chiplets provides enhanced operational characteristics with compact packaging. Chiplets from different vendors can be obtained from the open market, and then assembled and interconnected by the system integrator to build the final chip. However, the sheer complexity of the semiconductor supply chain makes the trust and assurance validation of chiplets extremely difficult. Previously, a physical inspection-based semiconductor certification authority (SeCA) was proposed for trust validation of chiplets which compares SEM images of chiplets and layout images, containing only active region information obtained from chiplet design houses, by using various image processing methods called the validation engine (VE). In this paper, we propose a VE architecture which uses statistical methods to determine the decision threshold and, hence, making the VE robust against local and global variations in the dataset. We have validated our proposed method to detect modified cells in 10 SEM images of 28 nm ICs.

P.38: Facilitating Assurance and Collaboration through Digital Threads in Microelectronics Experiments

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Laboratory experimentation with circuits and systems can be a complex process. Exact repetition of complex processes such as radiation testing, second-party verification of conclusions drawn from side channel analysis, and preservation of experimental processes all require the full detail of an experiment to be captured when it is run. Capturing a digital thread of an experiment provides this capability but can be a complex process that is prone to human error if not fully automated. This paper presents an automated microelectronics lab experimentation platform called Benches. We describe how Benches automates the capture of the digital thread of a microelectronics experiment and how these digital threads facilitate assurance and collaboration.

P.39: Generating Statistically Relevant Trojan Benchmarks for Microelectronics Quantifiable Assurance

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P.40: Multi-Tone Analysis for Authenticity of Electronic Devices

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P.41: ROPE: Re-usability LOck of Behavioral Intellectual PropErty

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High-Level Synthesis makes extensive use of synthesis directives that control how to synthesize mainly loops, arrays) and functions. This increases the re-usability of the behavioral code as it enables the generation of micro-architectures with different area vs. performance trade-offs. These advantages open the door to third party IP (3PIP) vendors providing Behavioral IPs (BIPs). Unfortunately, the market of third party BIPs is still

very small. Being so flexible is also their main weakness as it makes them only economically viable if the BIP provider can charge a large premium as it is highly unlikely that the BIP consumer will require their service again. Traditional IP vendors discriminate the price of the IP based on the amount of flexibility of the IP. We envision a similar price discrimination strategy for BIPs by limiting the re-usability of the BIP by partially encrypting the BIP source code.

P.42: Quantitative Information Flow Analysis of Hardware Designs Using Asset Flow Graphs

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An essential aspect of ensuring hardware security is to prevent the unauthorized disclosure of sensitive information. Such leakage can originate at either RTL or synthesized netlist abstraction levels due to design oversights or malicious insertion of leaky channels. Developing a unified information flow security verification framework that is applicable across both abstraction levels and a wide variety of threat models remains an unaddressed problem. A crucial step in developing such a framework is to anchor the leakage analysis through mathematically explainable metrics generalizable across different threat models and abstractions. In this paper, we introduce a novel end-to-end automatic information flow security (IFS) verification framework that tackles this problem by generating a graph representation of information flow of the design (called Asset Flow Graph). It utilizes this graph model to assign information theoretic entropy metrics to paths of the circuit and identify anomalous leakage channels without any assumptions on the source of the leakage or the structure of the circuit. Our experiments conducted on a wide variety of benchmark circuits proved the efficacy of proposed framework in detecting unauthorized information leakage.

P.43: Tamper Detection in Packaged Devices: Exhaustive Post-Silicon Verification Method Can Identify Hardware Trojan Attacks

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Despite significant industry and academic efforts to secure the semiconductor supply chain against tampering, including malicious attacks such as hardware trojans (HWT), few results have been shown to be effective or hold promise to date. However, a new approach based on a long forgotten “exhaustive verification” technique once used for printed circuit board (PCB) subassembly test shows promise together with modern cloud computing technology to non-invasively detect tampering in even the most advanced System-on-Chip (SoC) devices in their physical package. We have developed an automated test-based approach that allows the SoC owner to create a unique signature for their design before it leaves their secure facility for fabrication and then confirm that the resulting manufactured devices conform to that signature when returned to their lab for signature analysis. The approach promises to be highly effective against most HWT types when combined with industry-standard design-for-test (DFT) constraints.

P.44: Detection of Denial-of-Service Attacks in a Software-Defined LEO Constellation Network

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Satellite communication (SATCOM) is a critical infrastructure for tactical networks – especially for the intermittent communication of submarines. To ensure data reliability, recent SATCOM research has begun to embrace several advances, such as low earth orbit (LEO) satellite networks to reduce latency and increase throughput compared to long-distance geostationary (GEO) satellites, and software-defined networking (SDN) to increase network control and security. This paper proposes an SD-LEO constellation for submarines in communication networks. An SD-LEO architecture is

proposed, to Denial-of-Service (DoS) attack detection and classification using the categorical boost (CatBoost) algorithm. Numerical results demonstrate greater than ninety-six percent in accuracy, precision, recall, and F1-scores.

P.45: GLOBALFOUNDRIES GDSII Tape-In Structural Validation

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As microelectronics becomes integral to the economic vitality and security of this nation the dependency upon a secure and validated supply chain becomes a key concern. The semiconductor foundry is a complex operation across a multistage process with the customer design data, the processing of the design data, the delivery of the design data for masks, and then the processing steps to fabricate a state of art product. Through this process inherent risks exist regarding provenance, design and hardware integrity, confidentiality, and process control. The ability to confirm that an integrated circuit, especially a pre-designed circuit such as a pcell, has not been inadvertently or deliberately modified is an important task necessary to assure design and hardware integrity.

P.46: Sub-Micrometer Vibration Sensing Using a 0.4 THz Micro-Doppler Radar in 90 nm SiGe BiCMOS

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This paper presents a micro-doppler radar implemented using a 0.4 THz continuous wave (CW) silicon radiator. Sub-wavelength scale vibrations on a target can phase modulate an impinging THz wave. This phase modulation is detected and analyzed using interferometry, enabling the characterization of vibrations in the sub-micrometer scale. A sensitivity of 30 nm is measured, and measurement results using a CW monotone audio signal and speech is presented. Fabricated in GlobalFoundries 9HP 90 nm SiGe BiCMOS process, this chip consumes 70 mW.

P.47: Autonomous STAR Front-End with Intelligent Interference Correction

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Full duplex, or simultaneous transmit and receive (STAR) systems have become increasingly important as the frequency spectrum becomes more congested. One major issue with these systems is that self-interference (SI) occurs between the RX and TX paths. Many current STAR architectures that address SI do so at the cost of using bulky, expensive, or lossy devices. This work looks at a recently demonstrated STAR architecture, the quadrature balanced power amplifier (QBPA), which avoids the use of devices such as circulators and cancellers to more effectively cancel SI. Additionally, the QBPA is demonstrated with novel machine learning integration to maximize performance of the system when load variation and system behavior changes in real time.

P.48: MORA-Controlled 8 × 8 Antenna Switch

Jonathan Dixon, Nicholas Haglof, Nicholas Chillemi, James Martin, Richard Millard
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P.49: Dielectric Electromagnetic Sensor for Hostile Environments

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Young-Kai Chen
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This paper addresses the sensing of electromagnetic signals under harsh environments such as extremely high temperatures, intense ionizing plasma, geomagnetic storms, etc. Our technology platform utilizes metal-less dielectric antennas and passive optics in place of the conventional metallic RF antenna and interconnects, which are vulnerable to harsh environments. Additionally, with metallic losses being absent, the all-dielectric approach is well suitable for THz communication and sensing operations under intense plasmas.

P.50: Enabling Resilience Against Eavesdropping Attacks for Millimeter-Wave Antenna Arrays

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Antenna-array-based beamforming serves as the foundational technology for millimeter-wave (mmWave) wireless communications. In addition to combating the high path loss at mmWave, beamforming brings another benefit, which is greater resilience against eavesdropping. Despite the fact that most of the TX power is focused to the intended RX by the beamforming, there still exist leakages through array sidelobes, raising concerns for eavesdropping attacks in those directions. In this paper, we present a physical-layer security solution built upon recently developed antenna subset modulation (ASM) technique to protect mmWave TX from eavesdropping attacks. ASM scrambles the constellations outside the main lobe direction at each symbol transmission, thereby preventing information leakages through sidelobes. The unique advantage of ASM is that its power/area/design overhead is so small that every mmWave phased array can be potentially turned into an ASM transceiver without compromising the link distance, signal fidelity, or energy efficiency.

P.51: Wideband Frequency Selective Limiters for Communication Systems

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Frequency selective limiters (FSLs) based on the nonlinear magnetic phenomena in ferrites, enable frequency-selective power limiting of interference signals. The work described here, developed in-part during the DARPA M3IC program and continued in ONR Special Notice effort, is focused on the development of a wide-band, low power threshold, and surface mount FSL. These FSL devices can provide an automatic, self-adaptive frequency selective power limiting function that can protect the wide band communication receivers from high power saturation and damages.

P.52: A 1–3 GHz, 100-MHz BW Adaptive RF Self-Interference Cancellation IC for In-band Full-Duplex Radios

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Satheesh B. Venkatakrishnan
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This paper presents an 1–3 GHz RF self-interference cancellation (RF-SIC) design for in-band full-duplex radios. The design consists of a feedforward cancellation path between transmitter output and receiver input, which contains: 1) an adaptive analog finite-impulse response (FIR) filter with tunable delays; 2) a variable gain amplifier; 3) a clock generator. A reconfigurable

RF-SIC chip is fabricated using 45-nm SOI CMOS process. The measured amount of the SIC is more than 16 dB for a 100-MHz bandwidth modulated signal.

P.53: Intelligent Poly Key Zero Overhead Encode for Secure Communications

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Brennan Eveland
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Intelligent PolyKey (IPK) Zero Overhead Encode (ZOE) is a novel and secure method of encoding the data transmission between nodes on wireless and wired networks. The throughput energy per bit needed for the link is decreased by the gain of the forward error correcting code while the physical layer data is secured by constantly changing codes. This provides physical layer security because the transmitted symbols cannot be decoded from the noise without knowing a priori the current chosen Quasi-Cyclic Low Density Parity Check prototype matrix. The method was used to improve security and communications reliability with a Transpositional Modulation enabled system providing obfuscated communications and greater than 50% increase in data throughput.

P.54: A V-Band Downconversion Mixer in 90 nm GaN

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This paper presents a V-band downconversion mixer in 90 nm Gallium Nitride (GaN). This mixer uses low-side local oscillator (LO) injection to downconvert 50-61 GHz radio frequency (RF) signals to a 12.8 GHz intermediate frequency (IF). The LO input requires a 7dBm sinusoidal drive, and a single-balanced LO topology is implemented to improve the mixer's LO rejection. A novel Wilkinson-based LO to RF leakage cancellation circuit is implemented to provide a 22 dB isolation improvement at the mixer's RF input. A peak conversion gain of 12.6 dB and an average conversion gain of 5.3 dB is achieved. The average noise figure (NF) is 10.1 dB and output third-order intercept (OIP3) is 15.1 dBm. The mixer uses a 15 V drain supply and consumes 0.51 W. The design is currently being fabricated, with test results expected in early 2023.

P.55: Multi-Layer Fused Silica Processing for Millimeter-Wave Systems

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Shelby Nelson
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P.56: Dual-Band and Frequency-Reconfigurable Power Amplifiers

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This paper explores radio-frequency (RF) switch performance and its effects on frequency-reconfigurable and multi-band power amplifier (PA) topology selection. We describe the effects of a switch figure of merit (FOM) on the efficiency of the PA, compromises made due to parasitics within the switch transistor, and architectures that reduce or eliminate the need for RF switches. These studies were carried out in a hybrid circuit, 150-nm GaAs MMIC, and 150-nm GaN MMIC processes.

P.58: V-Band Transmit Phased Array for SATCOM Downlinks

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P.59: Useful Circuit Analogies to Model THz Field Effect Transistors

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Ultrafast 2D plasma effects for field-effect transistors (FETs) have been proven to help achieve terahertz operation from taking advantage of the breakup instability in the channel of the FET. Analytical models and calculations have been well developed while there is scarce circuit modeling efforts for this type of devices. Here, we demonstrate that analytical model calculations can be recovered by modelling THz FET using nanocavity, lossy transmission line and hybrid-pi like circuit analogies.

P.60: VLF Antenna Arrays for Efficient Subterranean and Underwater Wireless Communications

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Magnetoelectric (ME) antennas have recently been demonstrated as a promising solution for very low frequency (VLF) communications. In this work, a new type of ME antenna with high quality factor resonator is proposed to enhance the radiation field strength and efficiency. The radiation field was linearly increased with the number of antenna arrays. A total radiation field of 200 nT at 1 meter was achieved using 12 antenna arrays, which is one order of magnitude enhancement than a single antenna unit. Furthermore, the estimation of antenna efficiency based on the theory of magnetic dipole indicates that ME antennas can potentially enhance efficiency by a square law of the number of arrays. The demonstrated results and simulation analysis provide the potential for taking advantage of large number of ME antenna arrays for subterranean and underwater wireless communications.

P.61: Development of Low-Resistance Ohmic Contacts on N+ Phosphorous-Doped Diamond for Enabling High-Power Receiver-Protect Diodes

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We describe the development of low-resistance ohmic contacts on n+ phosphorous-doped diamond, which are critical for enabling high-power receiver-protect PiN diodes. Compared to the conventional materials used for commercially available high-power PiN diodes, diamond offers far superior materials properties for high-power limiter applications, with over 20× higher thermal conductivity. The power dissipation capability of these devices has also been found to exceed that of commercially available Si or GaAs diodes. The results presented provide a stronger fundamental understanding of n+ phosphorous-doped diamond growth and developing low-resistance ohmic contacts, which will guide future systematic parameter optimization for enabling high-performance RP PiN diodes, with superior power handling capabilities at a low system insertion loss.

P.62: Polarization-Graded III-N HEMTs for Highly Linear, High-Efficiency mm-Wave Transistors

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III-N-based HEMTs are leading candidates for high-performance millimeter-wave systems, with both excellent low-noise and high-power performance having been demonstrated. Despite this significant progress, recent theoretical and experimental work has demonstrated that further improvement in device linearity, power scaling, and power-added efficiency can be achieved using polarization-graded heterostructures. In contrast to conventional abrupt AlGaN/GaN heterostructure HEMTs, the use of polarization-engineered graded structures enables tailoring the transconductance and capacitance-voltage characteristics for improved linearity, enhances the channel carrier velocity, provides the ability to tailor the lateral electric field and enable higher voltage operation, and achieves high power-added efficiency. This promises to enable new levels of device performance to be achieved in GaN-based transistors.

P.63: Focusing and Diffraction of Light by Periodic Si Micropyramidal Arrays

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This research was devoted to modeling of the optical properties of Si micropyramids aimed at designing optimal structures for applications as light concentrators in mid-wave infrared (MWIR) focal place arrays (FPAs). It is shown that completely different optical properties of such structures can be realized using two types of boundary conditions (BCs): i) periodical and ii) perfectly matched layer. The first type (periodical BC) allowed us to predict the Talbot effect under plane wave coherent illumination conditions. This effect was experimentally demonstrated in the proposed structures. The second type (perfectly matched layer BC) allows describing the optical properties of individual micropyramids concentrating or “focusing” light on the photodetector. The optimal geometries of micropyramids required for maximizing the intensity of “photonic nanojets” emerging from their truncated tips are determined.

P.64: Hierarchical Device Planning for IC Packaging

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Intel, Newark, CA

Advanced IC Packaging design solutions are steadily evolving to support designer innovation on increasingly complex and high-capacity products. Yet its roots in PCB design are still visible where traditional IC Packaging

design solutions treat each device as a single flat entity. This makes it a challenge to optimize smaller functional areas of a BGA or co-designed IC and to reuse these areas in derivative designs. To address this challenge along with the inherent need to manage interface connectivity of a package device that is comprised of smaller building blocks, we introduce the concept of hierarchical device planning. This incorporates key hierarchical design methodology techniques – highly characteristic in chip design – into advanced IC packaging design.

P.65: Performance Metrics for Direct RF Transceivers: An Update to Traditional Metrics and Implementation Example

Marjorie Catt
Intel Programable Solutions Group, Champaign, IL

Dustin Henderson
Intel Programable Solutions Group, Berkely Heights, NJ

To achieve better RF performance, SWaP, and cost, both commercial and defense architectures have migrated from using separate IF ADCs and DACs to direct RF transceivers. To accurately evaluate the dynamic performance of a direct RF transceiver, it is necessary to revisit the traditional performance metrics used to evaluate IF data converters. This paper provides an in-depth analysis of direct RF transceiver performance evaluation, how the process differs from evaluating IF data converters, and implementation of an analysis platform.

P.66: A Near-Memory Accelerator for Real-Time Emulation of RF Interactions

Mandovi Mukherjee, Nael Mizanur Rahman, Sudarshan Sharma, Uday Kamal, Xiangyu Mao, Payman Behnam, Daehyun Kim, Jianming Tong, Jongseok Woo, Prachi Sinha, Coleman DeLude, Joseph Driscoll, Jamin Seo, Santosh Pande, Tushar Krishna, Justin Romberg, Madhavan Swaminathan, Saibal Mukhopadhyay
Georgia Institute of Technology, Atlanta, GA

P.67: Mixed-Signal Emulation for System-Level Performance Modeling of mm-Wave Direct Digital Beamforming Circuits

Lucas Duncan, Daron DiSabato, Tim Heaton, Tyler Heaton, Josef Danial
Niobium Microsystems, Dayton, OH

Jamin J. McCue
Air Force Research Laboratory, Wright-Patterson AFB, OH

P.68: An RTL-to-GDS Flow Based on an Industrial Electronic Design Automation (EDA) Toolchain for Single Flux Quantum Circuits

Eric Mlinar, Steve Whiteley, Anton Belov, Song Chen, Luca Amaru, Tong Liu, Yalan Zhang, Taufik Arifin, Min Pan, Troy Barbee, Rajinder Singh, Amir Ajami, Danny Rawlings, Arturo Salz, Robert Freeman, Scott Chase, Jamil Kawa
Synopsys, Inc., Mountain View, CA

Josephson Junction-based superconducting circuits are promising candidates for high-speed digital electronics with dramatically lower power consumption, as well as a key enabler in research towards the implementation of larger-scale quantum computing. In this paper, we demonstrate an automated flow for the creation of a microcontroller design, starting with a Register-Transfer Level (RTL) description of the circuit and completing with a candidate physical design for fabrication. We examine challenges specific to the superconducting electronics (SCE) technology at the different stages

in this flow, such as treatment of SCE libraries that contain a clock for all logic gates, the special placement demands on the clock tree for various SCE logic families, and other place-and-route considerations based on the SCE libraries and the foundry process features. We report on metrics to qualify the resulting physical layout, such as circuit density and timing results.

P.69: Automatic Modernization of Hardware Assets

Md Imtiaz Rashid, Amir T. Hossein, Benjamin Carrion Schaefer
University of Texas at Dallas, Richardson, TX

This work presents an RTL to C compiler that maximizes the re-usability of the generated C code for High-Level Synthesis (HLS). The uniqueness of the compiler is that it generates C code by using libraries of pre-characterized RTL micro-structures that are uniquely identifiable through perceptual hashes. This allows to quickly generate C descriptions that include arrays. loops and functions. These are important because HLS tools extensively use synthesis directives in the form of pragmas to control how to synthesize these constructs. E.g., arrays can be synthesized as registers or RAM, and loops fully unrolled, partially unrolled, not unrolled, or pipelined. Setting different pragma combinations lead to designs with unique area vs. performance and power trade-offs.

P.70: Modeling Graph Neural Networks for Gate Level Arrival Time Prediction of Long Tailed Datasets

Pratik Shrestha, Saran Phatharodom, Ioannis Savidis
Drexel University, Philadelphia, PA

An accurate estimate of the timing profile at different stages of the physical design allows for pre-emptive changes to the circuit, significantly reducing the design time and effort. In this work, a graph based deep regression model is utilized to predict the gate arrival time of the timing paths of a circuit. Three scenarios for post routing prediction are considered: prediction after completing floorplanning, after completing placement, and after completing clock tree synthesis. A commercial static timing analysis tool is utilized to determine the mean absolute percentage error (MAPE) and the mean absolute error (MAE) for each scenario. Results obtained across all trained models indicate that the proposed methodology outperforms the baseline errors produced by the commercial physical design tools with an average improvement of 62.82% in the MAPE score when predicting the post-routing arrival time after completing floorplanning and 17.8% improvement when predicting the post-routing arrival time after completing placement.

P.71: Balancing Performance and Power on the AI Edge

Gordon Cooper
Synopsys, Sunnyvale, CA

As AI implementations continue their move toward edge devices, there is a growing need for more efficient Neural Network processing across a broad range of performance, power and price points, leading to various processor-based implementation options. This paper will illustrate the trade-offs – including power and performance – between selecting an AI enabled DSP versus adding a dedicated AI accelerator including the newest Neural Processing Units (NPUs). Best practices in benchmarking will be covered and a review of use cases and the decisions made for applications including automotive, consumer and computer applications. The importance of software support across processors will also be covered.

P.72: A Comparative Study on DFTs in FPGA

Gregory Nash, Jody Forland
Intel PSG, San Jose, CA

This paper comprehends an efficient methodology and toolkit for implementing Discrete Fourier Transforms(DFTs) of arbitrary size, in Field Programmable Gate Arrays (FPGAs). Depending on application parameters, different approaches to the problem are required. Presented here

are three efficient algorithms including; a novel custom radix architecture, optimized radix 2^2 based FFT, and Bluestein's Chirp-Z algorithm. Simulation and timing analysis data is used to illustrate design trade offs between these methods for differing applications, and achievable performance using a wide range of transform sizes, while leveraging state of the art devices and development tools.

P.73: Ga_2O_3 Dielectric Heterojunction Diode with TiO_2 Interlayer for Reduced Leakage Current

Nolan Hendricks, Ahmad Islam, Kyle Liddy, Jeremiah Williams, Andrew Green
Air Force Research Laboratory, Sensors Directorate, Wright-Patterson AFB, OH

P.74: Microdose Effects of Neutron Radiation on 1200 V SiC Power n-MOSFETs

Christopher Stankus, Moinuddin Ahmed, John Hryn
Argonne National Laboratory, Lemont, IL

Stephen Arthur Wender, Kranti Gunthoti
Los Alamos National Laboratory, Los Alamos, NM

Commercial 1200 V SiC Power n-MOSFETs were subjected to reverse gate bias of 0–30 V_{SG} under neutron radiation. Devices were tested at 25 °C and 150 °C, with constant drain bias of 0 V, 50 V, and 100 V. Devices were exposed to an average fluence of 6.68×10^9 n/cm^2 above 1 MeV. Device current gate and drain current was monitored in situ during exposure. Devices experienced linear rise in source-gate current of 100 nA/V up to 25 V_{SG}, followed by apparent avalanche breakdown, with a maximum source-gate current of 4.0 μA. This linear current rise was unaffected by device temperature or drain voltage bias and persisted even when neutron radiation had ceased. Device behavior under radiation can be explained by neutron-induced ionization within the inherent gate-source diode of the device, as well as secondary ionization effects due to irradiation of device materials by neutron radiation.

P.75: Neutron Radiation In-situ Failure-in-time Characterization of 1200 V–1700 V SiC Power Transistors

Moinuddin Ahmed, Christopher Stankus, John Hryn
Argonne National Laboratory, Lemont, IL

Stephen Arthur Wender, Kranti Gunthoti
Los Alamos National Laboratory, Los Alamos, NM

This work is focused on the reliability testing of wideband gap (WBG) SiC power transistors due to terrestrial neutron radiation. Wide bandgap SiC power transistors are an attractive candidate for aerospace and satellite communication which offers a smaller footprint, lower weight, higher-temperature operation, lower power losses, and higher operating frequency. This work is a continuation of our earlier research. We have tested 1200 V–1700 V power transistors with/ without high temperature, and with/without angular placement in this work. The devices were in-situ tested for failure-in-time (FIT) analysis method at Los Alamos Neutron Science Center (LANSCE) in ICE House-1 facility at a flux of 10^6 n/cm^2-s above 1.5 MeV energy which is around 10^6 times higher than neutron radiation at airliner flight height.

P.76: A 3.7 V-to-1 kV Chip-Cascaded Piezo-Driver IC Achieving over 96% Reactive Power Efficiency

Yanqiao Li, Bahlakoana Mabetha, Jason T. Stauth
Dartmouth College, Hanover, NH

This work presents a modular/scalable switched capacitor (SC) converter with integrated auxiliary boost converter for high-voltage electrostatic and piezoelectric (PZT) actuators such as could be used for microrobotics, haptics and ultrasound applications. Allowing multiple chips to stack and

communicate across series voltage domains, with 3-chips stacked, the design interface from 3.7 V battery inputs to up to 1 kVpp (VCR > 270), delivering and recovering >1 W reactive power at >96% efficiency.

P.78: Optimizing New Power Switch Technology for Mil-Aero Applications: Packaging Development Process Yields First Working Double-sided Parts

Sam Sadri
QP Technologies, Escondido, CA

Jiankang Bu
Ideal Power, Inc., Austin, TX

Improving the efficiency and performance of semiconductor power switch components can have wide benefits, improving the efficiency and accelerating deployment of these applications for mil-aero and other markets. This paper studies the packaging challenges and the maturity cycle incurred for the B-TRAN™ double-sided power switch developed by Ideal Power, Inc., and provides the results achieved through the joint effort between Ideal Power and QP Technologies.

P.79: Fabrication Tolerant and Temperature Insensitive Photonic Circuit for Label Free Biosensing Applications

Sujith Chandran, Ramesh Kudalippalliyalil, Akhilesh Jaiswal, Ajey P. Jacob
University of Southern California, Marina Del Rey, CA

A microring resonator-based architecture is proposed for biosensing applications. For a specific use-case of Covid-19 detection, the proposed manufacturing compatible silicon photonics biosensor provides a spectral accuracy of <5 pm, better than conventional intensity-based detection schemes. Furthermore, our novel self-calibrating design addresses the temperature and fabrication sensitivity of state-of-the-art photonic sensors, paving the pathway for optical point-of-care biosensing.

P.80: Monolithic Integration of RF and Digital Electronics with Photonics for a High-Bandwidth Coherent Driver Modulator

Jacob Alward, Christian Bottenfield, Meredith Caveney, Christopher Coen, Christopher Curry, Michael Grady, Stephen Hurst, Paul K. Jo, Joji Joseph, Nelson Lourenco, Brandon Lovelace, Peter McMenamin, G. Joseph Samo, Leif Sandstrom, Billbang Sayasean, Nicholas Servies, Craig Swanson, Maxwell Tannenbaum, Brian Wier, Benjamin Yang, Anthony Zenere, Andrew Stark
Georgia Tech Research Institute, Atlanta, GA

Joshua Hawke
U.S. Naval Surface Warfare Center, Crane Division, Crane, IN

This paper describes GTRI's efforts to design, develop, and fabricate a custom system on a chip (SoC) for Department of Defense (DoD) applications based on an optical dual-parallel in-phase/quadrature (DP-IQ) modulator structure. This custom chip monolithically incorporates RF and digital electronics with photonic subcomponents as enabled by the choice of GlobalFoundries 45SPCLO fabrication process. The chip is packaged inside of a custom housing derived from the high-bandwidth coherent-driver modulator (HB-CDM) standard and then mounted on a 3U VPX circuit card assembly (CCA) for demonstration purposes.

P.81: A Single Chip K-band O-SSBM Using a Monolithically Integrated Quadrature Hybrid Coupler

Matthew Hagedon, Joseph Suelzer, Andrew Wegener
Air Force Research Lab, Sensors Directorate, Wright-Patterson AFB, OH

P.82: Intrinsic Warpage Problem Effects for Integrated Circuit Packages

ThuHong Tran
DoD, Fort Meade, MD

The electronics industry evolution has a flow out of handheld products, which have become essential components of our daily lives. As the end-product scaling for these microelectronic devices continues to shrink the dimension to fit into the portable market needs, our reliability concerns the intrinsic failure problem of short or open circuits, caused by the warpage deformation and solder joint crack. Since the DoD relies on commercial-off-the-shelf products, understanding these reliability concerns is essential to mission readiness. During high temperature stress test, the integrated circuit (IC) packages results in warpage deformation after 3D measurements. This change of the color mapping between the highest and lowest points reveals a warpage deformation for those IC packages. This might lead to an infant mortality problem for devices at the field. This poster provides scaling factors effects, different temperature test for various packages, contour observations, and discuss how avoid warpage problems for IC packages.

P.83: 3D Integration of Detector and ROIC through Wafer Bonding

Iqbal Ali, Brad Lenzen, Wey Lee, Hadrik Soni, Rafiqul Islam
Cactus Materials, Inc., Tempe, AZ

Highly segmented detectors with pixels smaller than 50 microns present a significant challenge for integration with arrays of thinned high density CMOS integrated circuits or Read Out Integrated Circuit (ROIC) chip with <50 microns thickness and areas of ~2 × 2 cm^2. Sensors can be built with large area (from 4 inch to 12 inch wafer) with good yield and high quality. This is not the case for readout chips, which are limited in size to the reticule (at most 3 × 2 cm) and have yields of at most 90–95%. The testing and placement yield of ROIC limits the size of an intelligent pixel array which can be produced efficiently. Since up to 5–10 connections per pixel between the readout high-density CMOS circuits and the detector may be required, bump bonding may not be up to the task. three-dimensional (3D) integration can address these challenges. A 3D integrated circuit is composed of multiple tiers of integrated electronics and sensors integrated vertically by hybrid bonding, thinning and insertion of through-silicon-vias (TSV).

P.84: Multi-Chiplet Implementation of a Replaceable Integrated Chiplet (PINCH) Assembly to Facilitate Heterogeneous Integration

Michael A. Nieves Calderon, Jonathan R. Brescia, Muhannad S. Bakir
Georgia Institute of Technology, Atlanta, GA

With the continuous growth of disaggregated systems, a need for new modular platforms to facilitate integration arises. A rePlaceable INegrated CHiplet (PINCH) assembly technology with the capability for reassembly, upgradeability, testing and prototyping systems of multiple chiplets at once is presented. PINCH consists of a socket platform, Positive Self-Alignment Structures (PSAS), Compressible Micro Interconnects (CMIs), and a glass interposer for die-to-die connectivity. The substrate agnostic PSAS-to-PSAS self-alignment technology allows us to get sub-micrometer alignment accuracy without the need of advanced alignment equipment. CMIs are non-permanent compliant off chip electrical interconnects with the capability of compensating for height differences and nonuniform assembly force. Two-dimensional arrays of 150 pitch CMIs are tested using the PINCH

assembly platform and four-point Kelvin resistance measurements are reported. To address the constant downscaling of interconnect dimensions and the increase in I/O densities, a two-dimensional 50 µm pitch CMI array is proposed, and preliminary simulation results are shown.

P.85: Mixed-Signal Spiking Neural Network for Energy-Efficient Computation

Sayma Nowshin Chowdhury, Sahil Shah
University of Maryland, College Park, MD

The abstract presents a hardware-aware modeling of mixed-signal circuits in a python framework. The work models analog synapses and mixed-signal neurons in python-based software framework. Current approach to training mixed-signal SNN or analog neural network is to learn the weights offline and then deploy them on hardware. In the case of mixed-signal hardware, the circuits employed for computation are non-linear and have significant variability. This work is initial work towards the goal of modeling this non-linearity and variability. The study uses Floating-Gate (FG) synapses for storing the weights of the synapses and adaptive Leaky-Integrate and Fire circuit for modeling the neurons in the SNN. Further, the study integrates a localized gradient-based algorithm to learn the FG voltage of the analog synapses of SNN. This approach enables integrating the non-linearity of analog synapses into the learning framework. Using these models and learning algorithm the work shows system-level classification using multiple layers.

P.86: Extremely Lightweight and Robust Insect-Drone Localization by Integrated Learning of Depth Estimates and Domain Map

Priyesh Shukla, Sureshkumar S., Amit R. Trivedi
University of Illinois at Chicago, Chicago, IL

Autonomy at insect-scale drones or ant-robotics is challenged by highly constrained resources. Robustness of tiny autonomous drones against domain variations is also critical. To address this, we propose extremely lightweight and robust localization at insect-scale drones by integrated learning of depth estimates and flying domain structure exploiting flying domain adaptability of DNN-based depth estimation and robustness of Bayesian particle filtering-based localization.

P.87: Automated Generation of Component-based Dataflow Accelerator for CNN on FPGAs

Danielle Tchuinkou Kwadjo, Christophe Bobda
University of Florida, Gainesville, FL

Developing a high-performance FPGA accelerator for CNN often demands high programming skills, hardware verification, accurate distribution localization, and long development cycles. Besides, CNN depth increases by reusing and replication of multiple layers. To the advantage of that property, this paper proposes a programming flow for CNN on FPGA to generate high-performance accelerators by assembling CNN pre-implemented components as a puzzle based on the graph topology. Using pre-implemented components allows us to use the minimum of resources necessary, predict the performance, and gain productivity since there is no need to synthesize any HDL code. Furthermore, components can be reused for a different range of applications. Through prototyping, we demonstrated the viability and relevance of our approach. Experiments show a productivity improvement of up to 69% compared to a traditional FPGA implementation while achieving over 1.75× higher Fmax with lower resources and power consumption.

P.88: Supervised Learning and Classification of Single-Event Transient Anomalies

Trevor Peyton, Berkay Dean, Jake Carpenter, Mohammed Fadul, Donald Reising, Daniel Loveless
University of Tennessee at Chattanooga, Chattanooga, TN

A convolutional neural network was designed to classify single-event transients based on the circuit node impacted by ionizing radiation. Nodes within a phase-locked loop are identified with over 90% accuracy as demonstrated through laser experiments.

P.89: Multiscale Modeling of Transition Metal Oxide (TMO) / Diamond Heterostructure

Mahesh R. Neupane
Army Research Directorate, DEVCOM Army Research Laboratory, Adelphi, MD
and
University of California, Riverside, CA

Pegah Mirabedini, Cameron Chevalier, Alex P. Greaney
University of California, Riverside, CA

Dmitry Ruzmetov, Pankaj B. Shah, James D. Weil, Derwin F. Washington, Stephen B. Kelley, Sergey Rudin, Leonard M. De La Cruz, Elias Garratt, A. Glen Birdwell, Tony G. Ivanov
Army Research Directorate, DEVCOM Army Research Laboratory, Adelphi, MD

Bradford B. Pate
U.S. Naval Research Laboratory, Washington DC

Diamond is an ultra-wide band gap semiconductor with exceptionally high thermal conductivity, which implies potential for superior performance and efficient thermal management of diamond RF transistors. High electrical conductivity in diamond can be achieved with surface transfer doping which has been shown to be enhanced by using transition metal oxides (TMO) as the surface acceptor layer. Vanadium Pentoxide (V_2O_5) is one of the commonly used TMO in surface doped diamond devices. In this study, we perform a multiscale modeling of V_2O_5/Diamond Heterostructure and analyze the structural and charge transfer dynamics by combining macroscopic, classical molecular dynamic simulation with atomistic, first-principal quantum mechanical simulation.

LUNCH **(12:00–1:30)**
Golden State Ballroom

T&AM-SPONSORED MPW OPPORTUNITIES

Thursday, 23 March / 10:30 am – 12:10 pm / Palms 4-6

The Trusted and Assured Microelectronics (T&AM) Program within OUSD Research & Engineering (R&E) aims to provide the U.S. warfighter with state-of-the-art (SOTA) assured microelectronics required to meet DoD system modernization goals. One of the primary objectives of the program is to enable access to commercial industry to develop and demonstrate SOTA designs that advance DoD initiatives. T&AM sponsors Multi-Project Wafer (MPW) run opportunities to enable access to SOTA US commercial foundries ≤ 22 nm in support of DoD microelectronics goals and to aid in developing DoD specific PDKs and IP. Currently, T&AM sponsors MPW opportunities with Global Foundries and Intel Foundry Services. The program is available to relevant designs from the defense industrial base (DIB), gov't labs, and academia. The panel will provide an overview of T&AM MPW opportunities and a discussion of technologies currently sponsored.

LUNCH **(12:00–1:30)**
Golden State Ballroom

Session 36

RF DESIGN TECHNOLOGIES AND TECHNIQUES

Thursday, 23 March / 1:30 – 3:10 pm /
Town and Country Ballroom A

Chair: **Steve Hary**
U.S. Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Tony Quach**
U.S. Air Force Research Laboratory, Wright-Patterson AFB, OH

36.1: Design-Technology Co-Optimization of Power Amplifiers for 5G Applications (1:30)

Nelson de Almeida Braga, Jonathan Cobb, Jingtian Fang, Ricardo Borges
Synopsys, Inc., Sunnyvale, CA

Binjie Cheng, Plamen Asenov
Synopsys Northern Europe Ltd., Glasgow, Scotland, UK

This paper describes an RF Technology-Design Co-Optimization (DTCO) simulation flow to support development of 5G, 6G hardware and other emerging wireless systems. The optimization flow includes Technology CAD (TCAD) simulations of fabrication processes and device electrothermal behavior, followed by extraction of SPICE compact models from TCAD results, and RF circuit-level simulations. A practical approach to assess root cause of non-linearities in Power Amplifiers is presented.

36.2: Linear, Efficient Multi-Carrier Envelope Tracking Power Amplifiers with Frequency Hopping for Phased Arrays 1:50 pm

Martin Navaroli, Paul Draxler, Dane Malangone, Eric Brown, Edward Falcon, Jonmei Yan
MaXentric Technologies, LLC, La Jolla, CA

An efficient, multi-carrier envelope tracking power amplifier system for next generation phased array applications, capable of frequency hopping over 500 MHz of bandwidth is presented with performance results. The system runs from a single FPGA and consists of four separate ETPA elements, each simultaneously amplifying a unique combination of two- to four-carrier aggregated signals that each span up to 500 MHz of overall bandwidth. The band-limited Adagio envelope shaping technique enables multi-carrier envelope tracking to enhance RF power amplifier efficiency, while novel digital pre-distortion algorithms that generate multi-waveform models were developed to enhance linearity over wide bandwidths. Each of the four sub-systems demonstrated post digital pre-distortion results for spectral regrowth of <-35 dBc, drain efficiency >35%, gain of 8 dB to 12 dB, and average output powers of 40 dBm to 43 dBm.

36.3: Device Figure of Merit for Load Modulated Power Amplifier Technology Selection (2:10)

Grant Giesbrecht, Taylor Barton
University of Colorado, Boulder, Boulder, CO

This paper describes a method for technology selection in high-frequency, energy-efficient poslackwer amplifier design. We describe two figures of merit that offer guidance in evaluating a technology's response over both frequency and load impedance. An example comparing two 150 nm GaN technologies shows that each has a frequency range where it may be preferred for a load-modulated power amplifier design.

36.4: Applying Machine Intelligence to Electromagnetic Field Estimations **(2:30)**

Yiliang Guo, Yifan Wang, Fnu Rahul Kumar, Rohit Sharma
Georgia Institute of Technology, Atlanta, GA

Joshua Corsello, Jeffery Logan, H. Bo Marr
Epirus Inc., Torrance, CA

Madhavan Swaminathan
Georgia Institute of Technology, Atlanta, GA
and
Penn State University, University Park, PA

In this paper a preliminary hybrid stochastic modeling approach is presented to rapidly predict spatial distribution of agile electromagnetic (EM) waveforms and the resulting internal electric fields when coupled into complex enclosures. The approach takes advantage of recent advancements in the numerical analysis and Machine Learning (ML) fields to provide high fidelity full volume results within 100s of milliseconds. Included in the approach are three unique models that are integrated into a hybrid framework: i) a fast time domain solver rapidly generates EM field training data, ii) a neural network provides rapid and generalized field predictions from training data, and iii) an optimization approach that identifies wave properties and/or designs to optimize electromagnetic fields throughout the enclosure. Preliminary results of this approach demonstrate full volume electromagnetic field estimations within complex enclosures with an average prediction accuracy exceeding 90% and 1,000× run-time improvements as compared to current commercial solvers.

36.5: High-Speed Compressive Sensing-Based Spectral and Angular Sensing with a Dual Mode Hardware Architecture **(2:50)**

Petar Barac, Peter R. Kinget
Columbia University, New York, NY

Matthew Bajor, Ronald Li, Constantine Pappas
Aspen Consulting Group, Sea Girt, NJ

Cognitive radio networks (CRN) rely on spectrum sensing and direction of arrival (DoA) estimation to operate dynamically in electromagnetic (EM) environments. CRNs can be used to determine which transceiver parameters are used to mitigate desensitization from interferers. Multi-antenna CRNs can additionally use beamforming to spatially filter interferers. Speed and accuracy are crucial factors for detecting and reacting to interferers. In this paper, the CRN utilizes an EM environmentally aware (EMEA) sensor to detect an interferer's spectral location and determine the DoA. The search is done in two domains: spectral and spatial. The sensing in each domain has been demonstrated to be ten times faster than the current state of the art. A custom RF-ASIC based on compressive sensing (CS) hardware architecture is used to perform rapid scans in sparse EM environments. Working in two domains offers an additional degree of freedom that improves the performance of cognitive radio architectures.

BREAK **(3:10–3:30)**

Session 37

ALTERNATIVE COMPUTING PARADIGMS

Thursday, 23 March / 1:30 – 3:10 pm /
Town and Country Ballroom B

Chair: **Cliff Lau**
Institute for Defense Analyses, Alexandria, VA

Co-Chair: **Sina Najmaei**
Army Research Laboratory, Adelphi, MD

37.1: GrapHD: Graph-based Hyperdimensional Memorization for Brain-Like Cognitive Learning (1:30)

Ali Zakeri, Zhuowen Zou, Mohsen Imani
University of California Irvine, Irvine, CA

Memorization is an essential functionality that enables today's machine learning algorithms to provide a high quality of learning and reasoning for each prediction. Memorization gives algorithms prior knowledge to keep the context and define confidence for their decision. Unfortunately, the existing deep learning algorithms have a weak and nontransparent notion of memorization. Brain-inspired HyperDimensional Computing (HDC) is introduced as a model of human memory. Therefore, it mimics several important functionalities of the brain memory by operating with a vector that is computationally tractable and mathematically rigorous in describing human cognition. In this manuscript, we introduce a brain-inspired system that represents HDC memorization capability over a graph of relations. We propose GrapHD, hyperdimensional memorization that represents graph-based information in high-dimensional space. GrapHD defines an encoding method representing complex graph structure while supporting both weighted and unweighted graphs. Our encoder spreads the information of all nodes and edges across into a full holistic representation so that no component is more responsible for storing any piece of information than another. Then, GrapHD defines several important cognitive functionalities over the encoded memory graph. These operations include memory reconstruction, information retrieval, graph matching, and shortest path. Our extensive evaluation shows that GrapHD: (1) significantly enhances learning capability by giving the notion of short/long term memorization to learning algorithms, (2) enables cognitive computing and reasoning over memorization graph, and (3) enables holographic brain-like computation with substantial robustness to noise and failure.

37.2: A 14 nm Stochastic-Compute-in-Memory Accelerator with In-Situ Stochastic Number Generator for Object Tracking Applications (1:50)

Jiyue Yang, Wojciech Romaszkan, Alexander Graening, Vinod Kurian Jacob, Tianmu Li, Puneet Gupta, Sudhakar Pamarti
University of California, Los Angeles, Los Angeles, CA

This work presents a stochastic compute-in-memory accelerator for object tracking applications. Stochastic computing uses tiny logic gates as the basic computation units and achieves massive on-chip parallelism to avoid unnecessary memory accesses. Previous stochastic compute-in-memory (SCIM) solutions rely on storing the entire bit stream representation of the binary numbers to perform the computation. Since an N-bit binary number requires at least 2^N stochastic bits to represent, it requires a large memory to store and degrades the throughput density (TOPS/mm^2). This work shows a SCIM solution that builds in-situ stochastic number generator inside the memory. Therefore, the memory only needs to store the binary number representation of the weights. The accelerator is designed in 14 nm and achieves 77 TOP/W energy efficiency for 6-bit compute and 13 TOPS/mm^2 throughput density.

37.3: Hyperdimensional Policy-based Reinforcement Learning for Continuous Control (2:10)

Mariam Issa, Yang Ni, Mohsen Imani
University of California Irvine, Irvine, CA

Traditional robot control or more general continuous control tasks often rely on carefully hand-crafted classic control methods. These models often lack the self-learning adaptability and intelligence to achieve human-level control. On the other hand, recent advancements in Reinforcement Learning (RL) present algorithms that have the capability of human-like learning. The integration of Deep Neural Networks (DNN) and RL thereby enables autonomous learning in robot control tasks. However, DNN-based RL brings both high quality learning and high computation cost, which is no longer ideal for currently fast-growing edge computing scenarios. In this paper, we introduce HDPG, a highly-efficient policy-based RL algorithm using Hyperdimensional Computing. Hyperdimensional computing is a lightweight brain-inspired learning methodology; its holistic representation of information leads to a well-defined set of hardware-friendly high-dimensional operations. Our HDPG fully exploits the efficient HDC for high-quality state value approximation and policy gradient update. In our experiments, we use HDPG for robotics tasks with continuous action space and achieve significantly higher rewards than DNN-based RL. Our evaluation also shows that HDPG achieves 4.7× faster and 5.3× higher energy efficiency than DNN-based RL running on embedded FPGA.

37.4: Near-Landauer Reversible Skyrmion Logic with Voltage-Based Propagation (2:30)

Benjamin W. Walker, Xuan Hu, Joseph S. Friedman
University of Texas at Dallas, Richardson, TX

Alexander J. Edwards
University of Texas at Dallas, Richardson, TX
and
Sandia National Laboratories, Albuquerque, NM

Michael P. Frank
Sandia National Laboratories, Albuquerque, NM

Felipe Garcia-Sanchez
Universidad de Salamanca, Salamanca, Spain

Magnetic skyrmions are topological quasiparticles whose non-volatility, detectability, and mobility make them exciting candidates for low-energy computing. Previous works have demonstrated the feasibility and efficiency of current-driven skyrmions in cascaded logic structures inspired by reversible computing. As skyrmions can be propelled through the voltage-controlled magnetic anisotropy (VCMA) effect with much greater efficiency, this work proposes a VCMA-based skyrmion propagation mechanism that drastically reduces energy dissipation. Additionally, we demonstrate the functionality of skyrmion logic gates enabled by our novel voltage-based propagation and estimate its energy efficiency relative to other logic schemes. The minimum dissipation of this VCMA-driven magnetic skyrmion logic at 0 K is found to be ~6× the room-temperature Landauer limit, indicating the potential for sub-Landauer dissipation through further engineering.

37.5: P^2M: Processing-in-Pixel-in-Memory Paradigm for Edge Intelligence **(2:50)**

Akhilesh Jaiswal, Peter Beerel, Ajey Jacob
University of Southern California, Los Angeles, CA

The demand to process vast amounts of data generated from state-of-the-art high-resolution cameras has motivated novel energy-efficient on-device AI solutions. Visual data in such cameras are usually captured in analog voltages by a sensor pixel array and then converted to the digital domain and transferred to cloud for subsequent AI processing, resulting in energy and throughput bottlenecks. To mitigate this problem, we propose a novel Processing-in-Pixel-in-memory (P^2M) paradigm that customizes the pixel array by adding support for analog multi-channel, multi-bit convolution, batch normalization, and ReLU (Rectified Linear Units). Our solution includes a holistic algorithm-circuit co-design approach, and the resulting P^2M paradigm can be used as a drop-in replacement for embedding memory-intensive first few layers of convolutional neural network (CNN) models within foundry-manufacturable CMOS image sensor platforms running state-of-the-art deep learning networks.

BREAK **(3:10–3:30)**

Session 38

SIDE-CHANNEL ANALYSIS

Thursday, 23 March / 1:30 – 3:10 pm /
Town and Country Ballroom C

Chair: **Greg Creech**
GLC Consulting, LLC, Columbus, OH

38.1: SCATE: Side Channel Analysis Testbench Emulator (1:30)

Jasper van Woudenberg, Rajesh Velegalati
Riscure, San Francisco, CA

Peter Grossmann
Zero ASIC Corp., Lexington, MA

Patrick Schaumont
Worcester Polytechnic Institute, Worcester, MA

Shreyas Sen
Purdue University, West Lafayette, IN

Side Channel Analysis (SCA) is an increasingly popular and increasingly inexpensive method for extracting keys from cryptographic implementations. Creating SCA-protected chips is non-trivial: it requires SCA experts at pre-silicon time, as well as multiple iterations where post-silicon analysis results improve the next tapeout. We propose an SCA vulnerability detection and countermeasure injection framework, which enables non-security-expert designers to create a side channel resistant design. The framework measures, ranks, and root causes SCA vulnerabilities in a design's RTL and netlist, allowing manual or automatic countermeasure addition. By virtue of the measurement and ranking, a designer can trade off the security target level with other overheads; this allows security to join power, performance, and area as optimization parameter in the ASIC design flow.

38.2: EMSC-GL: Security Assessment and Modeling of Electromagnetic Side-channel Leakage at Gate-Level (1:50)

Md Kawser Bepary, Tao Zhang, Kimia Zamiri Azar, Fahim Rahman, Farimah Farahmandi, Mark Tehranipoor
University of Florida, Gainesville, FL

In the modern electronic design flow, automation of security analysis is critical to identify and mitigate hardware vulnerabilities during the design phase. In this work, we propose an electromagnetic (EM) side-channel vulnerability assessment flow in the gate-level design stage that allows more flexibility to deploy countermeasures and decreases analysis cost and time compared to traditional layout-level or post-silicon analysis. This gate-level framework utilizes the register switching activity to account for the dynamic current flow and augments the model with empirical physical design-level data. Since the current flowing through the top metal layers significantly impacts the near-field EM emission, the distribution of interconnect metal layer is taken into consideration for model refinement. The Welch's t-test and Kullback-Leibler (KL) divergence metrics are computed with simulated traces to identify the EM side-channel vulnerability in the design. Experimental results from AES implementation exhibit the framework's effectiveness and provide insights into the rounds of operations.

38.3: Side-Channel Leakage of Flash ADC (2:10)

Ziyi Chen, Ioannis Savidis
Drexel University, Philadelphia, PA

In this paper, a monotonic power side-channel attack (PSA) is proposed to analyze the security vulnerabilities of flash analog-to-digital converters (ADC), where the digital output of a flash ADC is determined by characterizing the monotonic relationship between the power consumption traces and the applied input signals. A novel clock phase division technique is proposed to secure the power side channel information of a 4-bit flash ADC. The computation performed by the comparators of a flash ADC is divided into two distinct phases, which generate two power consumption peaks for each quantized digital output. The technique adds randomness to the power trace and decorrelates the input signal from the given power trace as the execution phase of a given comparator depends on the thermometer code computed from the last clock cycle. The overhead due to the protection circuitry is an additional 15 registers for a 4-bit flash ADC architecture. The monotonic PSA is performed for both a protected and unprotected ADC, with results indicating 1.9 bits of information leakage from the unprotected ADC and no data leakage from the protected ADC as the bit-wise accuracy is approximately 50% when secured. The monotonic PSA is more effective at attacking a flash ADC architecture as compared to either a convolutional neural network-based PSA or a correlation template PSA. The ADC core occupies an area of approximately 0.05 mm^2 in a 65 nm process, and provides a sampling frequency of up to 500 MHz at a supply voltage of 1.2 V.

38.4: Fast and Comprehensive Pre-Silicon Security Verification to Achieve Power Side-Channel Assurance (2:30)

Sreeja Chowdhury, Lang Lin, Jimin Wen, Hua Chen, Preeti Gupta, Norman Chang
Ansys, Inc., San Jose, CA

Kazuki Monta, Makoto Nagata
Kobe University, Kobe, Japan

Power side-channel attack utilizes transient power information from intellectual properties (IPs) to leak sensitive information from the design. These attacks are easy to implement, effective, low-cost, and non-invasive. Thus, it is a major concern in semiconductor security domain where it can cause potential leakage leading to massive security flaws. In this paper, we propose a fast comprehensive pre-silicon security verification flow targeting both register-transfer level (RTL) logic and gate design synthesis stages with record run-time which exposes the vulnerabilities existing in IPs. Our experiment shows that RTL flow can predict early architectural leakage whereas gate flow can estimate post synthesis leakage more accurately.

38.5: Determining Residual Risk from Optimized Selection of Hardware Trojan Detection Strategies (2:50)

Zachary Collier, Whitney Batchelor, Margaret Winslow, Scott Harper, Jonathan Graf
Graf Research, Blacksburg, VA

BREAK (3:10–3:30)

Session 39

GaN POWER ELECTRONICS

Thursday, 23 March / 1:30 – 3:10 pm /
Town and Country Ballroom D

Chair: **Travis Anderson**
U.S. Naval Research Lab, Washington, DC

Co-Chair: **Fritz Kub**
U.S. Naval Research Lab, Washington, DC

39.1: A GaN-HEMT Based High Power Cryogenically Cooled Converters : Challenges and Technical Gaps (1:30)

Yongduk Lee, Parag Kshirsagar
Raytheon Technologies Research Center, East Hartford, CT

This digest presents the development challenges and metrics for a high power cryogenically cooled power electronics converter. There is lots of challenges as follows: cryogenically cooled semiconductor devices, sub-circuit, cryogenic packaging, non-cryogenic device packaging and enclosure. Thus, this paper presents the technology gaps for the state of the art a cryo-cooled power electronic systems in the power density and cooling performance metrics required to enable the future electrified propulsion and defense systems. In the final manuscript, a cryo-cooled 2.5 MW power converter will be presented to evaluate a performance based on derived metrics and criteria. This is designed for commercial aerospace application through an ARPA-E funded program, it is broadly applicable for protection in naval power systems and other DoD applications and hence presented at this conference.

39.2: Mg Implantation for Selective Area p-type Doping of GaN and its Device Applications (1:50)

Spyridon Pavlidis, Shane R. Stein, M. Hayden Breckenridge, Shashwat Rathkanthiwar, Erhard Kohn, Ramón Collazo, Zlatko Sitar
NC State University, Raleigh, NC

Dolar Khachariya, William Mecouch, Seiji Mita, Baxter Moody, Pramod Reddy, James Tweedie, Ronny Kirste, Zlatko Sitar
Adroit Materials, Inc., Cary, NC

Kacper Sierakowski, Grzegorz Kamler, Michal Boćkowski
Polish Academy of Sciences, Warsaw, Poland

The enhanced critical electric field of GaN makes it an attractive technology for low-loss power devices. In order to fulfill its potential, selective area p-type doping via ion implantation is necessary. This manufacturing step has long been challenged by material decomposition at the temperatures needed for post-implantation activation annealing. In this work, we demonstrate how capless ultra-high pressure annealing for the effective repair of the GaN crystal and efficient activation of implanted magnesium. Following a materials-focused analysis of this process to identify optimal annealing conditions, we leverage Mg implantation and UHPA to demonstrate a 915 V GaN JBS diode with a specific differential ON-resistance of 0.6 $m\Omega \cdot cm^2$ and ideality factor of 1.03. These results ultimately demonstrate the potential of Mg implantation for future, high-performance GaN power devices.

39.3: Predicting Breakdown Failures in GaN Diodes Using Machine Learning Models with Optical Profilometry Data **(2:10)**

James Gallagher, Michael Mastro, Alan Jacobs, Karl Hobart, Travis Anderson, Mona Ebrish
U.S. Naval Research Laboratory, Washington, DC

Brendan Gunning, Robert Kaplar
Sandia National Labs, Albuquerque, NM

One major benefit of wide bandgap semiconductors such as GaN is the increased breakdown voltage at lower on-resistance. However, because GaN manufacturing is immature, wafers and epi layers often contain defects which can greatly lower the breakdown voltage, reducing the benefit of using GaN over more mature semiconductors such as Si or SiC. Many of these defects manifest as changes in the surface topography such as the presence of bumps or pits on the surface, which can be detected using optical profilometry. This research project focused on using machine learning algorithms to predict the probability of a GaN diodes undergoing low-voltage breakdown.

39.4: Impact of Anode Doping on Avalanche in Planar 1.2 kV Vertical GaN PiN Diodes **(2:30)**

Mona A. Ebrish, Alan Jacobs, James C. Gallagher, Karl D. Hobart, Travis J. Anderson
U.S. Naval Research Laboratory, Washington, DC

Matthew Porter
U.S. Naval Postgraduate School, Monterey, CA

Robert J. Kaplar, Brendan P. Gunning
Sandia National Laboratory, Albuquerque, NM

Vertical GaN PiN diodes with three different anode doping levels were fabricated on three wafers with the same p-layer thickness, and planar hybrid edge termination. A temperature dependent breakdown behavior were studied as functions of the anode doping, with the same anode thickness and fabrication sequence. The repeatable avalanche breakdown and highest breakdown voltage were measured with the moderate anode doping level of 1×10^{18} cm^{-3}, indicating the efficacy of the Nitrogen implanted hybrid edge termination design that comprises of junction termination and guard rings hybrid design. As the anode doping increases the remaining dose in the termination region increases, and the devices exhibit lower breakdown voltages and less robust breakdown characteristic, often destructive. From this study, we also conclude that both a very high p-layer doping of 2×10^{19} cm^{-3} and a low p-layer doping of 5×10^{17} cm^{-3} are not practical doping levels as they are too sensitive to the edge termination thickness.

39.5: Experimental Demonstration of GaN Super-Heterojunction MOSFETs with 3 kV Dynamic Switching and 10 kV Blocking **(2:50)**

Jesse T. Kemmerling, Rian Guan, Mansura Sadek, Yixin Xiong, Jianan Song, Sang-Woo Han, Rongming Chu
Pennsylvania State University, University Park, PA

This is a report of an experimental demonstration of lateral GaN MOSFETs with dynamic switching characterized up to 3 kV and blocking voltage measured up to 10 kV. The highvoltage capability was achieved by implementing the GaN Superheterojunction (SHJ) design, which flattens the E-field profile between the gate and the drain. The GaN SHJ-MOSFETs showed scaling of blocking voltage with the SHJ length up to 10 kV, low static on-resistance of 81.6 Ωmm or 84.2 $m\Omega cm^2$, as well as controlled dynamic on-resistance degradation of 123 percent when switched from an off-state bias of 3 kV.

BREAK **(3:10–3:30)**

Session 40

ADVANCED COMPONENTS

Thursday, 23 March / 1:30 – 3:10 pm / Palms Room 1-3

Co-Chair: **Saverio Fazzari**
Booz Allen Hamilton, Clarksville, MD

40.1: A 4 GHz-to-8 GHz High Resolution Inverter Based Vector Modulator in Low Voltage 12 nm FinFet (1:30)

Mehdi Abderezai
HRL, El Segundo, CA

Chris M. Thomas
Boeing BR&T SSED, El Segundo, CA

Mehdi Katoozi
Boeing BR&T SSED, Seattle, WA

A broadband high resolution four-channel vector modulator is presented as the basis for a quadrature clock calibration block in a low voltage high precision I/Q quadrature digital synthesizer. Each channel of the vector modulator is comprised of a digitally controlled multi-stage “inverter based” phase modulator and duty cycle correction. The vector modulator was fabricated in a 12 nm FinFet CMOS process achieving an operating range of 4 GHz to 8 GHz, an Image Rejection Ratio (IRR) of 60 dBc at 8 GHz, a power consumption of nominally 50 mW, and an active area of 280 um × 180 um.

40.2: P^2M: Processing-in-Pixel-in-Memory Paradigm for Edge Intelligence (1:50)

Akhilesh Jaiswal, Peter Beerel, Ajey Jacob
University of Southern California, Los Angeles, CA

The demand to process vast amounts of data generated from state-of-the-art high resolution cameras has motivated novel energy-efficient on-device AI solutions. Visual data in such cameras are usually captured in analog voltages by a sensor pixel array, and then converted to the digital domain and transferred to cloud for subsequent AI processing, resulting in energy and throughput bottlenecks. To mitigate this problem, we propose a novel Processing-in-Pixel-in-memory (P^2M) paradigm, that customizes the pixel array by adding support for analog multi-channel, multi-bit convolution, batch normalization, and ReLU (Rectified Linear Units). Our solution includes a holistic algorithm-circuit co-design approach and the resulting P^2M paradigm can be used as a drop-in replacement for embedding memory-intensive first few layers of convolutional neural network (CNN) models within foundry-manufacturable CMOS image sensor platforms running state-of-the-art deep learning networks.

40.3: Highly Accurate Voltage Reference for High Precision Applications **(2:10)**

Bryce Gadogbe, Randall Geiger, Degang Chen
Iowa State University, Ames, IA

A strategy for designing a highly accurate voltage reference operating at sub 1 ppm over a wide temperature range is proposed. The proposed design makes use one of the common and widely used BJT-based voltage reference structure and the temperature dependence of the drain current of a single MOS transistor operating in subthreshold to build a highly accurate voltage reference for high precision applications. The effects of error sources which may affect the performance of the voltage reference are analyzed and minimized. Simulation results in the TSMC 180 nm process show that the design can achieve temperature coefficients of less than 1 ppm/°C across process corners and local random variations from -40 °C to 125 °C after trimming.

40.4: Non-volatile Memory Circuit with Self-Terminating Read Current **(2:30)**

Sarah R. Evans, Mitchell J. Rickard, Aric Fowler, Yiorgos Makris, Naimul Hassan, Alexander J. Edwards, Disha Biswas, Joseph S. Friedman
University of Texas at Dallas, Richardson, TX

Conventional approaches for reading the resistance of non-volatile memory devices require constant current flow and power dissipation, thereby preventing the continuous reading of non-volatile memory with less energy than static random-access memory (SRAM). We propose a self-terminating read mechanism that enables continuous reading of the non-volatile memory state without requiring continuous current flow. This approach enables circuits that are robust to power cycling and consume 20× less energy than SRAM and 5–10× less energy than a non-volatile memory voltage divider circuit.

40.5: Neural Network Calibration of 6 GS/s 8-channel CIC SAR Time-Interleaved ADC **(2:50)**

Michael Flynn, Evelyn Ware, Justin Correll, Seungjong Lee
University of Michigan, Ann Arbor, MI

An area efficient time-interleaved charge-injection-cell SAR ADC is enabled by neural-network calibration. The prototype time-interleaved ADC interleaves 8 CIC SAR channels for a total sampling rate of 6 Gs/s. The area is only 0.00608 mm^2. The neural network calibration algorithm corrects multiple error sources in the time-interleaved ADC. The ADC is fabricated in 28 nm CMOS. The neural calibration method effectively improves the average measured resolution of the time-interleaved ADC from 4.1 bits to 5.5 bits.

BREAK **(3:10–3:30)**

Session 41

RF SYSTEMS

Thursday, 23 March / 3:30 – 5:10 pm /
Town and Country Ballroom A

Chair: **Thomas Dalrymple**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Mark Yeary**

41.1: **Flight Test Results for Ultra-Long Endurance UAS Low-Cost Direction-Finding Sensor Payload** **(3:30)**

Jonathan Dixon, Nathan Blood, Nicholas Haglof, Nicholas Chillemi, Colin McLaughlin, David Smart, Richard Millard
SI2 Technologies, Inc., North Billerica, MA

Dave Curtis, Mike Bryant, Mike Minardi, Kris Kim, Alex Burwell, Damon Kelly, Colin Beck, Karleigh Pine, Andrew Homan, Matt Ferrara
Matrix Research, Inc., Dayton, OH

Adam Propst, Jonathan Washburn, Jonathan Rasche, Anthony Jones, Dan Edwards
Platform Aerospace, Inc., Hollywood, MD

Jay Weitzen
University of Massachusetts Lowell, Lowell, MA

41.2: **Extremely Wideband RF Spectrum RF Operations (EWO) Proof of Concept Testbed** **(3:50)**

Jose Torres, M. Wajih Elsallal, Stanley Chien, Ken Schmitt
MITRE Corporation, Bedford, MA

A new class of wideband phased array, radio frequency (RF) personality, and a heterogeneous field-programmable gate array (FPGA) equipped with integrated and more efficient data converters are being developed to demonstrate spectrum agility and provide high-speed data throughputs in contested environments. This wideband digital phased array is powered by direct RF conversion architecture, operating over a 2–18 GHz spectrum with more than 2 GHz instantaneous signal bandwidths with a sample rates up to 64 GSPS. The testbed was used as a showcase for multi-RF function (sensing, communications, and EW) capabilities in mission relevant environments.

41.3: Millimeter-wave and IR Multimodal Sensing System Enabling AI-based Event Recognition with Enhanced Privacy (4:10)

Asaf Tzadok, Stanislav Lukashov, Alberto Valdes-Garcia
IBM T. J. Watson Research Center, Yorktown Heights, NY

Technologies for sensing and monitoring human-related activities and vehicles/objects are an important and increasing part of urban management and safety. It is desirable to enable these systems to operate without visible-domain cameras for enhanced privacy and robustness to varying illumination and weather conditions. In response to these requirements, we introduce a multimodal sensing system that comprises 60-GHz phased array TX and RX modules, a passive IR camera, a COTS-based FMCW radar sub-system, a mixed-signal data acquisition module, and an FPGA. The FPGA's key role is to accurately control radar waveform generation, phased array beam steering, and IR camera data acquisition events, producing a synchronized high-speed stream of 3D radar (>3 Kfps) and IR (9 fps) data. The prototype system and an associated multi-modal DNN are evaluated in two use cases (1) concealed object detection and (2) head gesture classification.

41.4: Demonstration System for Advanced Waveforms, Digital Beamforming and Digital Building Blocks (4:30)

Amanda Panneton, Seth Lipko, Fadi Afiouni
Northrop Grumman Corporation, Linthicum, MD

Thomas Dalrymple, Peter Buxa, Matt Longbrake
Air Force Research Laboratory, Wright-Patterson AFB, OH

41.5: Scalable Ka-band SATCOM Transmit Ground Terminal with 48 dBW EIRP and High XPD (4:50)

Kevin K. W. Low, Gokhan Gultepe, Qian Ma, Gabriel M. Rebeiz
Extreme Waves, Inc., San Diego, CA

Ka-band satellite communications (SATCOM) offers a high data rate internet service and gets more and more resilient as its global coverage is expanding. This paper presents a scalable a Ka-band transmit SATCOM ground terminal with state-of-the-art performance. The planar phased-array achieves an EIRP of 47–48 dBW at 27.5–30 GHz and can close a link in satellite constellations while meeting off-axis EIRP spectral density (ESD) mask requirements. The phased-array can operate in any polarization state with a cross-polarization discrimination (XPD) above 20 dB due to a dual-polarized antenna design driven by active, gain and phase adjustable channels. Also, due to its symmetrical design, it requires only a single point calibration for all scan angles, simplifying system design and operation.

Session 42

RF FILTERS AND CANCELLERS

Thursday, 23 March / 3:30 – 5:10 pm /
Town and Country Ballroom B

Chair: **Timothy Hancock**
Raytheon Technologies, Tewksbury, MA

Co-Chair: **Nelson Lourenco**

42.1: An All-Analog Signal Conditioner for On-Aperture STAR Applications (3:30)

Nelson E. Lourenco, Christopher T. Coen, Douglas R. Denison, David Landgren, Jeramy Marsh, Charlie Hunter, Connor Frost, Matthew Tate
GTRI Advanced Concepts Laboratory, Atlanta, GA

An all-analog feed-forward isolator capability is demonstrated that enables integration of isolation enhancing electronics directly on an antenna backplane, using novel wideband (2–20 GHz) finite-impulse response (FIR) monolithic microwave integrated circuits (MMIC) realized in SiGe. This architecture will enable array antennas to support simultaneous transmit and receive by enabling sub-partitions that each transmit or receive (respectively) without interfering with each other.

42.2: A Magnetostatic Spin Wave-based Analog Frequency Selective Canceller for Interference Excision (3:50)

Reena Dahle, Scott Gillette, Michael Geiler, David J. Audette, Anton L. Geiler
Metamagnetics, Inc., Marlborough, MA

A magnetostatic spin wave-based analog frequency selective canceller (FSC) that exhibits a novel reference-free cancellation method has been successfully demonstrated. Unlike traditional fixed and/or tunable notch filters, active beam nulling, and solid-state limiters, this FSC improves receiver front end capability by automatically rejecting threats (in-band, modulated, blocker, etc.) while simultaneously enabling reception of signals of interest (SOI). The FSC technology utilizes our frequency limiting (FSL) technology, the Auto-tune Filter (AtF), and leverages its attributes to enable automatic rejection of above-threshold electromagnetic interferers without the need for any reference or sample of the interferer. This FSC has many applications including being placed pre-or post-LNA, and it can be integrated into a system in such a means that it can be called upon when needed (e.g., switchable function on OpenVPX card).

42.3: Autonomously Tunable Interference Tracking Filter (AITF) for Wideband Direct Sampling Receiver (4:10)

Sanghoon Shin, Hans Haucke
U.S. Naval Research Laboratory, Washington, DC

42.4: Next Generation BAW Filters for AESAs (4:30)

Ralph Rothemund, Mudar AlJoumayly
Qorvo Inc., Apopka, FL

Recent advances in Bulk Acoustic Wave (BAW) filters enable extending the operating spectrum to cover X- and Ku-bands. This paper presents an overview of BAW resonator and filter design to develop high frequency applications and demonstrate its power handling capabilities. Switched filter bank architectures for phase array antenna applications is also presented.

42.5: Contiguous, Constant Bandwidth and Reconfigurable Bandpass Filter Using SLCFET Technology (4:50)

Matthew Torpey, Robert S. Howell
Northrop Grumman Mission Systems, Linthicum, MD

We report on the successful fabrication and demonstration of a low loss, high performance constant bandwidth, contiguous, and reconfigurable bandpass filter technology of a digitally reconfigurable bandpass filter. The same circuitry was implemented in both a commercial GaAs pHEMT process as well as Northrop Grumman's GaN based SLCFET technology. The resulting filter operates between 1.0–2.0 GHz, with over 500 different filters of variable center frequencies and variable bandwidths from 70 MHz to 1400 MHz, all in a single device. The SLCFET filters demonstrated a NF and insertion loss improvement over the GaAs variant by >2 dB, and $P1dB_{average}$ of 33.6 dBm, compared to an average $P1dB_{average}$ = 17.8 dBm power handling of the GaAs filter. The SLCFET based filter was measured as having 20× greater linearity than the GaAs filter, with the average two tone IIP3 for the SLCFET filter at 43 dBm, compared to 30 dBm.

Session 43

PROTECTION METHODS & ASSESSMENTS

Thursday, 23 March / 3:30 – 5:10 pm /
Town and Country Ballroom C

Chair: **Michael Wehrmeister**
National Security Agency, Fort Meade, MD

43.1: I'm Reading Your Obfuscated Design and You Can Too (3:30)

John Haussermann
Department of Defense, Fort Meade, MD

Assume that an integrated circuit design contains secrets. Assume that it is unacceptable that anyone analyzing the integrated circuit design learn those secrets. Designers of Logic Locking and Logic Obfuscation techniques have recently claimed some of those techniques to be sufficient to protect secrets in circuit designs from analysis efforts. They claimed efficacy comparable to NIST-approved crypt algorithms. Reviews of some of these Logic Locking and Logic Obfuscation techniques found those claims to be false. In some cases these techniques were circumvented by the naked eye. In this presentation, some of the common major shortcomings in Logic Locking and Logic Obfuscation will be discussed. Recommendations will be made about what serious research into the feasibility of Logic Locking and Logic Obfuscation for protecting secrets would look like.

43.2: Red Teaming Methodology for Design Obfuscation (3:50)

Yuntao Liu, Abir Akib, Zelin Lu, Qian Xu, Ankur Srivastava, Gang Qu,
University of Maryland, College Park, College Park, MD

David Kehlet, Nij Dorairaj
Intel Corporation, San Jose, CA

The main goal of design obfuscation is to protect sensitive design details from being obtained by untrusted parties in the VLSI supply chain, including but not limited to off-shore foundries and untrusted end users. In this work, we present a systematic red teaming approach to evaluate the security of design obfuscation approaches. Specifically, we consider the scenario where the adversary does not have access to a working chip, and propose security metrics and an evaluation methodology to assess the effectiveness of obfuscation. A case study on Ripper, the obfuscation scheme used in the State-of-the-Art Heterogeneous Integrated Packing (SHIP) program, indicates that the leaked design information is more than commonly expected, which suggests that the security of Ripper needs to be improved.

43.3: OASIS: A Layered IP Protection Framework for Structured ASIC (4:10)

Rasheed Almawzan, Reiner Dizon-Paradis, Aritra Dasgupta, Dipal Halder, Md Moshiur Rahman, Maneesh Merugu, Sandip Ray, Swarup Bhunia
University of Florida, Gainesville, FL

Kostas Amberiadis
Intel Corporation, Santa Clara, CA

Due to globalization and inexpensive labor, electronics companies are heavily relying on third-party sources for most of the fabrication process, including new technologies like structured ASIC. Consequently, IP designers have considered a zero-trust model, where the attacker is assumed to have access to IP design at any stage. However, the existing body of work has not addressed shortcomings in structured ASIC and is only designed against a small subset of attack surfaces. In this work, we propose a multi-layered approach for protecting confidentiality and integrity attacks using a synergistic combination of countermeasures over two abstraction levels to address this issue in structured ASIC. The shortcoming of any countermeasure is rectified by the other security mechanisms in the proposed approach. The layered approach in the proposed approach also makes the implementation suitable for structured ASIC, where the unused resources in configurable logic blocks are utilized to minimize overhead costs.

43.4: ATPG and Test Methods for Redacted IP (4:30)

Jackson Fugate, Greg Stitt, Naren Vikram Raj Masna, Aritra Dasgupta, Swarup Bhunia
University of Florida, Gainesville, FL

Nij Dorairaj, David Kehlet
Intel Corporation, Santa Clara, CA

Automated test-pattern generation (ATPG) is a critical part of verifying post-fabrication hardware. One limitation of existing ATPG methods is that they are specialized for fixed-logic designs where the application functionality is provided to the ATPG tool. This use case conflicts with an emerging trend to redact security-critical IP via reconfigurable hardware, whose specific functionality is only known after providing a bitstream that is serially loaded into a set of configuration flip-flops. Using existing ATPG methods to test a redacted design provides testing times that are 12.5× to 19.3× longer than the original design. In this paper, we explore novel ATPG strategies for redacted IP to maximize stuck-at fault coverage, while minimizing testing time. We show significantly improved testing times that are between 1.8× and 2.2× slower than the unredacted designs, without requiring any knowledge of the original design, and while integrating more easily into design-for-testability flows than existing eFPGA approaches.

43.5: Countering Reverse Engineering and Cloning in Heterogeneously Integrated Systems (4:50)

Md Saad Ul Haque, Fahim Rahman, Farimah Farahmandi, Mark Tehranipoor
University of Florida, Gainesville, FL

Heterogeneous integration (HI), has become an attractive alternative to minimize the limitations of System on Chip (SoC) technology like costs, yield loss, performance, etc. Although the industry is currently transitioning towards HI, many design and security challenges associated with advanced packaging yet remain unaddressed. This paper presents a detailed vulnerability assessment of system-level reverse engineering, and IP Piracy inherent in the HI domain and the applicability of the existing countermeasures in monolithic SoC. Based on that, we propose an adaptable multi-tiered mitigation approach using logic locking and physical design obfuscation. We also analyze the security of our countermeasures concerning logistic attacks and brute-force attempts by potential adversaries.

Session 44

RADIATION HARDENED CHARACTERIZATION MECHANISMS

Thursday, 23 March / 3:30 – 4:50 pm /
Town and Country Ballroom D

Chair: **Daniel Loveless**
University of Tennessee at Chattanooga, Chattanooga, TN

Co-Chair: **Jon Ahlbin**
Vanderbilt University, Nashville, TN

44.1: Detecting Radiation-aware Functional Safety Violation via Early Anomaly Detection (3:30)

Ayush Arunachalam, Kanad Basu
University of Texas at Dallas, Richardson, TX

The proliferation of safety-critical applications in the automotive and space domains has resulted in ensuring the functional safety of Electrical and/or Electronic (E/E) systems that constitute systems in these domains. The analog and Mixed-Signal (AMS) circuits that constitute such systems are more susceptible to faults than their digital counterparts due to exposure to external radiations. In this work, we propose a novel unsupervised learning framework, which leverages the continuous signal properties of these AMS circuits, to perform early anomaly detection. The proposed approach involves the generation of a comprehensive anomaly training dataset in various circuit locations and components, feature extraction from observation signals, and clustering algorithms to enable anomaly detection. The anomaly detection performance is further improved and expedited by incorporating time series analysis. Our experimental results demonstrate the effectiveness of our solution, furnishing up to 100% accuracy. Furthermore, the time series approach reduces the anomaly detection latency by 5×.

44.2: Towards Radiation-aware Functional Safety in Online AI Accelerators (3:50)

Shamik Kundu, Kanad Basu
University of Texas at Dallas, Dallas, TX

Drastic technology scaling in recent years has made custom-built AI inference accelerators highly vulnerable to faults, engendering from impingement of high-energy radiation particles. Such faults are detrimental to the classification accuracy of the AI accelerator, leading to the critical Functional Safety (FuSa) violation, when used in mission-critical applications. In order to detect such violations in mission mode, we analyze the efficiency of a software-based self test scheme that employs functional test patterns, akin to instances in the application dataset. Such patterns are either selected from the dataset of the Deep Neural Network (DNN), or generated from scratch utilizing the concept of Generative Adversarial Networks (GANs). When evaluated on state-of-the-art DNNs on multivariate exhaustive datasets, the GAN generated test patterns significantly improve FuSa violation detection coverage by up to 130.28%, compared to the selected test patterns, thereby accomplishing efficient testing of the AI accelerator, online, in mission mode.

44.3: GaN Vacuum Nanoelectronics for Radiation Hardened Devices (4:10)

George Wang, Keshab Sapkota, A. Alec Talin, Francois Leonard, Gyorgy Vizkelethy
Sandia National Laboratories, Albuquerque, NM

The III-nitride semiconductors are attractive for solid-state vacuum nanoelectronics, having high thermal and chemical stability, low electron affinity, and high breakdown fields. Here we report top-down fabricated, lateral gallium nitride (GaN)-based nanoscale vacuum electron diodes operable in air, with ultra-low turn-on voltages down to ~0.24 V, and stable high field emission currents, tested up to several microamps for single-emitter devices and up to the mA level for arrayed devices. We present gap-size dependent and pressure dependent studies which provide insights into the design of future nanogap vacuum electron devices. Device characteristics after proton, electron, and neutron irradiation will be discussed. The results show promise for a new class of robust, integrated, III-nitride based vacuum nanoelectronics that may be inherently radiation hard.

44.4: Radiation Effects on Vertical β-Ga_2O_3 Power Diodes (4:30)

Esmat Farzana, Arkka Bhattacharyya, James S. Speck
University of California Santa Barbara, Santa Barbara, CA

Nolan S. Hendricks
University of California Santa Barbara, Santa Barbara, CA and
Air Force Research Laboratory, Wright-Patterson AFB, OH

Rick M. Cadena, Dennis R. Ball, Sajal Islam, Aditha S. Senarath, Enxia Zhang, Daniel M. Fleetwood, Ronald R. Schrimpf
Vanderbilt University, Nashville, TN

Vertical Beta Gallium Oxide Schottky Diodes were investigated in this work under heavy ion and alpha particle irradiation. The heavy-ions resulted in early catastrophic device breakdown which was suggested to cause by the ion-induced high local electric field from TCAD simulation. Based on the results, improved leakage management was performed in the diodes combining high Schottky barrier contact with oxidized metals and high dielectric constant field plate towards development of radiation–hard devices.

Session 45

LEADING EDGE DESIGN

Thursday, 23 March / 3:30 – 5:10 pm / Palms Room 1-3

Chair: **Julian Warchall**
Booze Allen Hamilton

Co-Chair: **Wes Hansford**
Boeing, Huntington Beach, CA

45.1: 5 nm 256 Kb Secure Read Only Memory (ROM) (3:30)

Eric Hunt-Schroeder, Darren Anand, Steven Lamphier, Sundar Sankarasubramanian, Dale Pontius, Girish Nair, Darrin Hinterneder
Marvell Semiconductor, Burlington, VT

Designed and manufactured in TSMC 5nm FinFET technology is a 256 Kb Secure Read Only Memory (ROM). Unlike a conventional ROM that stores data with a via connection, this Secure ROM uses two mismatched threshold voltage NFETs (twin-cell) to store data securely. Differential current sensing is used to briefly determine the data stored when sensed and maintains secure data at rest at all other times. The Secure ROM supports 0.675 V to 0.96 V at-circuit voltages and temperatures of –40 °C to 125 °C. A time zero (T0) test screen using a current imbalance while sensing reduces test time and can predict early end of life failures from insufficient differential signal with natural aging effects in CMOS devices.

45.2: Direct RF FPGAs with Integrated 64 GSPS Data Converters (3:50)

Benjamin Esposito
Intel Programmable Solutions Group, San Jose, CA

Conor O Keeffe, Carmine Pagano, John Rucki
Intel Programmable Solutions Group, Cork, Ireland and San Jose, CA

45.3: Robust and Efficient Genome Sequence Matching on Emerging Processing In-Memory Platform (3:50)

Zhuowen Zou, Hanning Chen, Mohsen Imani
University of California Irvine, Irvine, CA

Prathyush Poduval
University of Maryland, College Park, MD

Rosario Cammarota
Intel Labs, San Diego, CA

In this paper, we propose BioHD, a novel genomic sequence searching platform based on Hyper-Dimensional Computing (HDC) for hardware-friendly computation. BioHD transforms inherent sequential processes of genome matching to highly-parallelizable computation tasks. We exploit HDC memorization to encode and represent the genome sequences using high-dimensional vectors. Then, it combines the genome sequences to generate an HDC reference library. During the sequence searching, BioHD performs exact or approximate similarity check of an encoded query with the HDC reference library. Our framework simplifies the required sequence matching operations while introducing a statistical model to control the alignment quality. To get actual advantage from BioHD inherent robustness and parallelism, we design a processing in-memory (PIM) architecture with massive parallelism and compatible with the existing crossbar memory. Our PIM architecture supports all essential BioHD operations natively in memory with minimal modification on the array. We evaluate BioHD accuracy and efficiency on a wide range of genomics data, including COVID-19 databases. Our results indicate that PIM provides 102.8× and 116.1× (9.3× and 13.2×) speedup and energy efficiency compared to the state-of-the-art pattern matching algorithm running on GeForce RTX 3060 Ti GPU (state-of-the-art PIM accelerator).

45.4: Reimagine Case Study: Design of a 6 Billion Transistor SOC with a Small Team (4:30)

Matthew Stamplis, Ana-Maria Mandrila Vacca, Jonathan Leu, Anythony Kryzak, Richard Younger, Jon Frechette
MIT Lincoln Laboratory, Lexington, MA

45.5: Reusing, Not Reinventing, the Wheel: A Study of the Design, Fabrication, and Integration of a Custom Chiplet for Solving Signal Processing Limitations for Commercial and National Security Applications (4:50)

Cayley Rice, Michael Roeder
Leidos, Inc., San Diego, CA

By leveraging commercial advances in microelectronic design process, tools, and IP our small team successfully fabricated a 12 nm, 4B+ transistor signal processing chiplet. As much as possible of the chiplet to test board integration process uses domestic sources, demonstrating and testing an on-shore supply chain for similar advanced microelectronics. We present lessons learned to demonstrate a viable approach to dual-use microelectronics to support adoption and expansion of the chiplet ecosystem and advance microelectronics available for DOD missions.

Session 46

SOLID STATE TECHNOLOGY FOR PULSED POWER

Thursday, 23 March / 3:30 – 5:10 pm / Palms 4-6

Chair: **Joseph Croman**
Navy Research Laboratory

Co-Chair: **Travis Anderson**
U.S. Naval Research Laboratory, Washington, DC

46.1: High Voltage Pulse Sharpening with Semiconductor Closing Switches **(3:30)**

Andrew Koehler, Joseph Croman, Karl Hobart, Rachael Myers-Ward, Travis Anderson
U.S. Naval Research Laboratory, Washington, DC

Geoffrey Foster
Jacobs Inc. Residing at NRL, Washington, DC

Kindred Griffis
University of California Davis, Davis, CA

A semiconductor closing switch (SCS) evaluation circuit is constructed to characterize SCSs for high voltage pulse sharpening applications. Design considerations for SCS devices are discussed in order to achieve kilovolt switching, with subnanosecond rise times.

46.2: Design Consideration for 10 kV Si and SiC Avalanche Sharpening Diodes **(3:50)**

Reza Ghandi
GE Research Center, Niskayuna, NY

Jason Sanders
Transient Plasma Systems, Inc., Torrance, CA

In This report, MIXED-MODE modeling of Si and SiC avalanche sharpening diodes are presented. Also, design consideration for 10 kV Si and SiC sharpening diodes is discussed. Si diodes require a stack of at least 5 diodes to achieve 10 kV sharpening operation. However, a single junction SiC diode can generate 10 kV pulse without the need for stacking devices.

46.3: DSRD Research at LLNL **(4:10)**

Caitlin Chapin, Sara Harrison, Laura Leos
LLNL, Livermore, CA

Mark Rader
SMDC, Hunstville, AL

This talk will present recent progress on DSRDs and related devices at LLNL.

46.4: Stacked Diodes for Pulsed Power Applications: New Process Integration Scheme **(4:30)**

A. Usenko, A. N. Caruso, S. Dhungana, R. Allen
University of Missouri-Kansas City, Kansas City, MO

S. Bellinger
Semiconductor Power Technologies, Manhattan, KS

Since Boff, Moll, and Shen's discovery of the high-speed switching effect inherent in initially forward-biased silicon diodes that are suddenly reverse-biased in 1960; DSRD's (as termed by Grekhov and Kardo-Sysoev in 1985) performance has not increased as their deep-diffusion manufacturing process remains the same as it was over 60 years ago. Albeit new pulse generator topologies which utilize diodes like DSRDs, i.e., SOS diodes (termed by Rukin in 1992) have shown improvement at circuit level given they operate under a higher direct-current density compared to that of DSRD-based pulsers – the voltage-to-risetime, dV/dt, of these silicon-based solid-state diodes remain on the order of 10E12 V/s. Furthermore, all possible ways to improve pulse performance of DSRD made by deep diffusion have been extensively investigated and exhausted. To achieve the 10E13 V/s (10 kV/ns) voltage-to-risetime required by an all-solid-state pulse generation utilized to support of the missions, improving DSRD manufacturing techniques must ensue.

46.5: Characterization of a GaN-based Photoconductive Semiconductor Switch for Power Electronics **(4:50)**

Geoffrey Foster
Jacobs Inc., Hanover, MD

Andrew Koehler, Karl Hobart, Travis Anderson
U.S. Naval Research Lab, Washington, DC

Raghav Khanna
University of Toledo, Toledo, OH

Semi-insulating, carbon-doped gallium nitride is an excellent candidate for a photoconductive switch. The energy levels from the carbon-related defects allow photocurrent generation from near to above band gap light. By utilizing a high-powered commercial off-the-shelf (COTS) light emitting diodes (LED), low on-resistance is demonstrated with high breakdown voltage, outperforming conventional GaN devices along the Baliga figure of merit.

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