GOMACTech-06

Government Microcircuit Applications
and
Critical Technology Conference

ADVANCE PROGRAM

"Exploring Invisible Worlds "

March 20 – 23, 2006

Paradise Point Resort
San Diego, California

GOMACTech-06
ADVANCE PROGRAM
CONTENTS

WELCOME

The GOMACTech-06 Program Committee is pleased to welcome you to this year's conference in San Diego, California. GOMACTech is the pre-eminent conference for the review of developments in microcircuit applications for government systems. Historically, the Conference has been the venue to announce major government microelectronics initiatives such as VHSIC, MIMIC, and others. GOMACTech was established in 1968 and is an Unclassified, Export-Controlled event that requires all participants to be U.S. Citizens or legal U.S. Permanent Residents.

This year's conference theme, "Exploring Invisible Worlds," provides a forum for discussing and demonstrating recent breakthroughs in our capability for precision measurements. Humankind has always been characterized by exploration. Early explorers moved in the world on a geographical scale, mapping the land and seas by hand. As technology advances, so does the precision of measurement, which expands our capability for exploration out to the reaches of the universe and into the realm of the atom.

This year's conference will follow a format that has proven very successful in recent years, in which both technical and topical sessions will be included. The technical sessions will consist of papers that are both contributed and solicited, while the topical sessions will consist of presentations that are focused on the work being performed within selected ongoing government-sponsored programs. Topical session themes this year include Electronic and Photonic Integrated Circuits, Nanotechnology for Systems, Radiation-Hardened Microelectronics Roadmaps (Government and Industry), Vertically Integrated Sensor Arrays, and Wide-Bandgap Semiconductors.

On Tuesday morning, the conference will formally begin with an outstanding Plenary Session. Major General Roger A. Nadeau, Commanding General, U.S. Army Research, Development and Engineering Command (RDECOM), will present the keynote address. In keeping with the conference theme, the Jack Kilby Lecture Series will feature Dr. Nader Engheta of the University of Pennsylvania who will be presenting "Seeing the Invisible: Polarization Vision in Nature and Non-Invasive Imaging and Sensing Applications." As a tribute to Jack Kilby, Dr. Jim Van Tassel will present a special remembrance of Mr. Kilby's life and contributions.

Prior to the formal opening of the conference, two tutorials will be offered on Monday afternoon with the cost included as part of the conference registration fee. In the first tutorial, *THz-Frequency Sensing for the Future*, expert researchers from academic and government laboratories will provide overviews of recent progress in science and technology for sensors in the Terahertz region of the spectrum. In the second tutorial, *Nanotechnology,* leading technologists from academia and industry will provide an overview of nano-sensor technology progress and potential.

The Plenary and Technical Paper Sessions are the major sources of formal information exchange that will occur at the conference. Other sources are provided through the Exhibitors that include major IC manufacturers and commercial vendors of devices, equipment, systems, and services for nearly all facets of the electronics business. The exhibition opens on Tuesday at noon and runs through Wednesday at 4:00 pm. An Exhibitors' Reception, sponsored by Northrop Grumman, where attendees can mix in a relaxing atmosphere of food and good spirits will be held on Tuesday evening. On Thursday, a Government

Applications and Vision Session will be held during lunch in which current and future directions of government-sponsored programs will be presented.

This year's strong technical program reflects the hard work of the GOMACTech-06 Technical Program Committee. The committee aggressively sought out particular topics and areas for presentations, and the quality of the conference will positively reflect this effort. We appreciate your support and believe that GOMACTech-06 will be a rewarding experience.

Sammy Kayali
Conference Chair

Dev Palmer
Technical Program Chair

REGISTRATION

All sessions of GOMACTech-06 are being held at the Paradise Point Resort & Spa in San Diego, California. Both check-in and on-site registration will take place in the hotel's Paradise Ballroom Foyer.

Conference check-in and on-site registration hours:

Monday, 20 March – 10:00 am – 5:00 pm
Tuesday, 21 March – 7:00 am – 5:00 pm
Wednesday, 22 March – 7:00 am – 5:00 pm
Thursday, 23 March – 7:00 am – 5:00 pm

SECURITY PROCEDURES

The GOMACTech Conference is an Unclassified, Export-Controlled event that requires participants to be U.S. Citizens or legal U.S. Permanent Residents. All registrants must provide proof of U.S. Citizenship or Permanent Resident status prior to being permitted entry into the conference. Additionally, a signed **Non-Disclosure Statement** will be required.

You may prove U.S. citizenship with any one of the following:
U.S. Passport
Birth Certificate **AND** valid government-issued photo ID
Naturalization Certificate **AND** valid government-issued photo ID

The following are NOT proof of citizenship:
Voter registration card
Driver's license

GOMACTech TUTORIALS

Two tutorials of interest to the GOMACTech community are a special feature of the conference. There is no additional fee for the tutorials but registrants must indicate their intention to attend on the registration form.

Tutorial 1: Nano-Sensor Technology

Monday, March 20, 1:00 – 6:00 pm
Dockside Room

Moderators:
Louis Lome, Institute for Defense Analyses, Alexandria, VA
Joe E. Brewer, University of Florida, Melrose, FL

Rapid progress in nanotechnology has enabled the creation of a new generation of sensors that permit the detection of a wide range of physical and chemical phenomena and are compatible with implementation of highly integrated subsystems. These miniature devices promise to greatly expand the range of affordable analysis systems, and enable the creation of greatly improved and more comprehensive capabilities in medical, defense and commercial systems. This tutorial is intended to provide an overview of nanosensor-technology progress and

potential. It is not a tutorial in the classical sense of a textbook-type mode of presentation. It consists of seven presentations by leading technologists from universities and industry who are working on different aspects of nanosensors.

Tutorial 2: THz-Frequency Sensing for the Future

Monday March 20, 10:00 – 5:30 pm
Bayview Room

Moderator: Dwight Woolard
U.S. Army Research Office, Research Triangle Park, NC

In recent years, the field of terahertz (THz) science and technology has entered a completely new phase of unprecedented expansion that is generating ever-growing levels of broad-based international attention. One can legitimately argue that that the potential payoffs of THz sensing (and imaging) to applications areas such as defense, security, biology, and medicine are the major drivers of this new phenomenon. However, there remain major science and technology (S&T) "gaps" within the THz regime that must be reconciled before many of the perceived payoffs ever become realizable. This tutorial will present a number of talks on leading research efforts that are attending to close the S&T gaps with the long-range goal of enabling future sensing (and imaging) applications with relevance to the military and private sectors.

EXHIBITION

An exhibition comprised of commercial vendors exhibiting products of interest to the GOMACTech community is an integral part of the conference. All attendees are reminded to visit the exhibit hall when they have some free time. The Exhibit Hall is located in the hotel's Paradise Ballroom. Coffee breaks will be held in the exhibit area when they coincide with the exhibition's hours of operation. On Tuesday evening an Exhibitors' Reception will be held, sponsored by the Northrop Grumman, where attendees can mix in a relaxing atmosphere of food and good spirits. Exhibition hours are as follows:

Tuesday, 21 March	12:00 pm – 8:00 pm
Wednesday, 22 March	9:00 am – 4:00 pm

Exhibitors

ATK Mission Research

JSI Microelectronics

M/A-COM

Northrop Grumman

Sandia National Laboratories

The Boeing Company

WEDNESDAY EVENING SOCIAL AT SEA WORLD

This year's Wednesday Evening Social Event will be held at SEA WORLD, the world's premier marine life park, located on beautiful Mission Bay. We will be greeted by one of Sea World's costumed characters and receive a personalized admission ticket and a custom printed program. We will then be escorted for a Reception at Wild Artic and a Dinner at the Nautilus Pavilion. Wild Arctic, an unprecedented attraction, features a breathtaking simulated helicopter flight over the frozen north. But the excitement doesn't end there. After disembarking, you will enter Base Station Wild Arctic, a realistic center for polar exploration that features above-water- and underwater-viewing of polar bears, beluga whales, walruses, and harbor seals. This attraction captures the beauty and starkness of the Arctic environment. As you journey through this frozen wonderland, you will see polar bears forage, walruses hauling themselves out onto ice floes, and beluga whales gazing through the glass. It's an adventurous expedition through an area of the world few have experienced before. The evening will conclude with a half-hour private Dolphin Discovery Show.

Bus transportation will be provided.

Tickets should be purchased in advance along with your conference registration. Adults $25; Children (12 and under) $15.

HOTEL ACCOMMODATIONS

It's Southern California, just as you've pictured it – blue skies, towering palms, and a landscape exploding with color. And it's all here outside your plush, single-level bungalow. Step onto your lanai to find cloudless skies, lapping waves, soft sand beaches, and lush gardens. Sound like paradise? You may just have found it at Paradise Point Resort & Spa – a private 44-acre island tucked away on gentle Mission Bay, minutes from the heart of San Diego.

GOMACTech has reserved a block of rooms at the hotel at a special rate of $169 single/double. These rates are exclusive of California Transient Accommodations tax (currently 10.7%). Overnight parking is $18/night.

To ensure the group rate, just log on to www.paradisepoint.com, click on make a reservation and fill in your arrival and departure dates and in the box marked Group/Event ID enter the code no. 25639. Or, you can call the hotel reservation office at 1-800-344-2626.

Reservations received after the February 24th cut-off date will be accepted on a space and/or rate availability basis only.

CONFERENCE CONTACT

Anyone requiring additional information about GOMACTech should contact the Conference Coordinator, Ralph Nadell, GOMACTech, 411 Lafayette Street, Suite 201, New York, NY 10003 (212/460-8090 x203), Rnadell@pcm411.com.

GOMACTech '05 PAPER AWARDS

Paper awards based on audience evaluations from GOMACTech-05 will include the George Abraham Outstanding Paper Award, two Meritorious Paper Awards, and a Best Poster Paper Award. Presentation of these well-deserved awards will be made at the Plenary Session on Tuesday morning in the Sunset II Ballroom. The GOMACTech-05 winners are:

The George Abraham Outstanding Paper Award (5.4)

Y. Afridi, A. Hefner, C. Ellenwood, R. Cavicchi, and S. Semancik, NIST, Gaithersburg, MD
"*Characterization System for Embedded Gas Sensor Systems-on-a-Chip (SOC)***"**

Meritorious Paper Award (9.3)

T. H. Meng and B. Murmann, Stanford University, Stanford, CA
"*Digitally Assisted Analog Circuit Design for Communication SoCs*"

Meritorious Paper Award (14.2)

J. Palmour, Cree, Inc, Durham, NC
"*A Roadmap of Silicon-Carbide Power Devices*"

Best Poster Paper Award (P.6)

K. A. LaBel and M. J. Sampson, NASA/GSFC, Greenbelt, MD
C. E. Barnes, Jet Propulsion Laboratory, Pasadena, CA
"The NASA Electronic Parts and Packaging (NEPP) Program: Roadmap for NASA's Radiation Effects on and Reliability of Electronics Efforts."

QUESTIONNAIRE

Don't forget to complete your questionnaire before you leave the conference. The questionnaire will be handed out at conference check-in. To encourage submission of this form, GOMACTech has a special gift for all attendees submitting a completed form. Please turn your form in at the Conference registration desk when you leave the Conference to receive your gift item.

SPEAKERS' PREP ROOM

Executive Suite 701 is designated as a speakers' prep room and will be available during the hours the conference registration desk is open. Speakers are encouraged to use the Executive Suite 701 facilities to ensure compatibility with the meeting's AV equipment. Speakers having difficulties should request at the conference registration desk to see an AV operator. Speakers are also asked to be at their assigned presentation room 30 minutes before the sessions begins to meet with their session chair. An AV operator will be assigned to each technical session room.

CD-ROM PROCEEDINGS

A volume of the GOMACTech-06 CD-ROM Proceedings, containing searchable, condensed versions of submitted papers presented at the Conference will be distributed to all registrants. Additional copies of the CD-ROM can be purchased at the Conference at a cost of $40.00 per CD.

Previously published as the GOMAC Digest of Technical Papers, Volumes I – XXVII, this publication is the only record of the conference. Previous GOMAC Digests will, upon request, made available copies to qualified Defense Technical Information Center (DTIC) users. Please call 1-800-225-3842 for bound or microfiche copies. Past Digests can be ordered by calling the above number and identifying the following accession numbers (please note that GOMAC was not held in the calendar year of 1995):

GOMAC-84 B113271	-86 B107186	-87 B119187
-88 B129239	-89 B138550	-90 B150254
-91 B160081	-92 B169396	-93 B177761
-94 B195015	-96 B212362	-97 B222171
-98 B235088	-99 B242763	-00 B254138
-01 B264749	-02 B275146	-03 M201604
-04 M201663	-05 M201849	

INFORMATION / MESSAGE CENTER

The Information/Message Center will be located adjacent to the GOMACTech Registration Desk in the Paradise Point Resort. The message center telephone number for incoming calls is 858/274-4630. Callers should ask to be transferred to the GOMACTech Registration Desk.

PARTICIPATING GOVERNMENT ORGANIZATIONS

Participating Government Organizations of GOMACTech-06 include: Department of Defense (Army, Navy, Air Force) ... National Aeronautics and Space Administration ... Department of Commerce (National Institute of Standards and Technology) ... National Security Agency ... Department of Energy (Sandia National Laboratories) ... Defense Logistics Agency ... Department of Health and Human Services ... Defense Threat Reduction Agency ... Advisory Group on Electron Devices ... Defense Advanced Research Projects Agency ... Central Intelligence Agency ... National Reconnaissance Office

GOMAC WEB SITE

Information on GOMACTech may be obtained through its Web site at www.gomactech.net.

TUESDAY

Session 1

PLENARY SESSION

Tuesday, 21 March / 9:00 am – 12:00 pm / Sunset II Ballroom

Opening Remarks **(9:00–9:15)**

Sammy Kayali, GOMACTech-06 General Chair
Jet Propulsion Laboratory, Pasadena, CA

GOMACTech Awards **(9:15–9:30)**

Keynote Address **(9:30–10:30)**

Major General Roger Nadeau
Commander, U.S. Army Research, Development and Engineering Command, Aberdeen Proving Ground.

To be announced

BREAK **(10:30–11:00)**

Jack S. Kilby Lecture Series **(11:00–12:00)**

Prof. Nader Engheta
University of Pennsylvania, Department of Electrical and Systems Engineering, Philadelphia, PA

"***Seeing the Invisible: Polarization Vision in Nature and Non-Invasive Imaging and Sensing Applications***"

Dr. James H. Van Tassel
Bonita Springs, FL

"***Jack Remembered***"

LUNCH **(12:00–1:30)**

SESSION 2

MEMS DEVICES AND APPLICATIONS

Tuesday / March 21 / 1:30 – 3:00 pm / Room 1

Chair: **Eric D. Adler**
Army Research Laboratory, Adelphi, MD

Co Chair: **William D. Palmer**
U.S. Army Research Office, Durham, NC

2.1: **Tailoring Capacitive Switch Technology for Reliable Operation** **(1:30)**

C. Goldsmith and D. Forehand
MEMtronics Corp., Plano, Texas

X-B. Yuan and James Hwang
Lehigh University, Bethlehem, PA

Recent developments in dielectric charging and switch design methodologies which enable capacitive-like proximity switches to operate without the failure modes normally associated with capacitive switches and dielectric charging will be examined. The discussion will also include the challenges of demonstrating high cycle life times and potential methods for accelerated testing.

2.2: **Ultra-High-Sensitivity MEMS-Based Optical Displacement Sensor** **(1:50)**

R. L. Waters, H. F. Jazo. M. S. Fralick, and T. E. Jones
SPAWAR Systems Center, San Diego, CA

An ultra-high-sensitivity MEMS-based displacement sensor has been fabricated based on the monolithic integration of a Fabry–Perot interferometer and a photodiode. Experimental measurements have yielded displacement sensitivities as small as 10 fm per root Hz. This measurement has also been shown to be consistent with the Heisenberg uncertainty principle.

2.3: **MEMS Tunable 4–16-GHz Notch Filters** **(2:10)**

R. M. Young, J. D. Adam, T. T. Braggins, and H-K. Hahn
Northrop Grumman Corp., Baltimore, MD

Two tunable notch filters covering 4–16-GHz with a 1–2-dB out-of-band insertion loss, each having 16 (4 bit) tuning states matching 3-D simulations will be demonstrated. All matching and impedance transformation occurs on the 3×3 mm^2 chip, needing only dc input voltages to set MEMS capacitance switch arrays to the chosen filter state.

2.4: **Demonstration of a Ku-Band RF MEMS-Enabled Electronically Scanned Antenna** **(2:30)**

D. Judy, S. Weiss, R. Polcawich, and J. Pulskamp
Army Research Laboratory, Adelphi, MD

An overview of the Army Research Laboratory's design, fabrication, and measurement of an eight-element Ku-band rf MEMs-based electronically scanned antenna (ESA) will be presented. The effort resulted in successful beam steering using rf MEMs-based phase shifters. The work represents the Army Research Laboratory's continuing effort in low-cost electronically scanned antennas in support of the Future Force.

BREAK **(3:00–3:30)**

Session 3

DISTRIBUTED AUTONOMOUS SENSORS: SYSTEMS, SUBSYSTEMS, AND EXPERIMENTATION

Tuesday / March 21 / 1:30 – 3:00 pm / Room 2

Chair: **Jill P Dahlburg**
Naval Research Laboratory, Washington, DC

Co-Chair: **B. Kiviat**
Naval Research Laboratory, Washington, DC

3.1: **Wolf PAC: Command and Control of Geographically Dispersed Networked Forces** **(1:30)**

G. Glaros
OSD, Force Transformation, Arlington, VA

The Office of Force Transformation (OFT) is undertaking an initiative – Wolf PAC – to explore command and control of geographically dispersed, networked, autonomous, and semi-autonomous assets. Forces are becoming increasingly burdened by the lack of a coherent strategy to "control" large numbers of dispersed assets. Distributing those assets geographically, loosely federated by networks, only serves to increase the complexity of these controlling challenges.

3.2: **CDP: A Spectral–Temporal Sensor for Energetic Events** **(1:50)**

R. J. Nelson and J. M. Mooney
Solid State Scientific Corp., Nashua, NH

F. Barone
Naval Research Laboratory, Washington, DC

D. Leahy
Air Force Research Laboratory. Bedford, MA

The Crossed Dispersion Prism (CDP) sensor represents a new class of spectral-temporal sensing device. The sensor measures the spectral–temporal profile of un-cued dynamic energetic events, such as explosions or plumes, for discrimination and identification purposes. Applications include missile threat warning, battlefield preparation, and real-time bomb-damage assessment.

3.3: **Use of the JPL Electronic Nose to Detect Leaks and Spills in an Enclosed Environment** **(2:10)**

M. A. Ryan, M. L. Homer, H. Zhou, and C. R. Lewis
Jet Propulsion Laboratory, Pasadena, CA

The use of an array of polymer-based chemical sensors in the JPL electronic nose to detect, identify, and quantify chemical events caused by specific compounds in a complex background will be discussed. The discussion includes sensor selection for the detection of inorganic and organic species and approaches which can be used for near real-time data analysis.

3.4: Photonics Sensors for Chemical and Biological Agents Detection **(2:30)**

R. Dutt and J. Chan
APIC, Culver City, CA

A laser photoacoustic spectrometer (PAS) system for detection of chemical agents, explosive residues, and narcotics and a biosensor chip has been developed. In the PAS system, the most important component is the tunable photonic source. The integration of solid-state LWIR lasers and quantum cascade lasers (QCLs) allows us to achieve a significant performance improvement over first-generation PASs that use lasers with more-limited operating ranges. A biosensor chip based on silicon-on-insulator (SOI) photonics integrated circuits (PICs), which leads to low-cost and small-sized biological/chemical agent detection system, has also been developed. A roadmap for further miniaturization will be discussed.

BREAK **(3:00–3:30)**

Session 4

RF MICROSYSTEMS AND PACKAGING

Tuesday, March 21 / 3:30 – 5:00 pm / Room 1

Chair: **William D. Palmer**
U.S. Army Research Office, Durham, NC

Co-Chair: **Eric D. Adler**
Army Research Laboratory, Adelphi, MD

4.1: Micro-Electromagnetic rf Systems (3:30)

D. Filipovic
University of Colorado, Boulder, CO

G. Potvin and D. Fontaine
BAE SYSTEMS, Merrimack, NH

Revolutionary research developing low-loss high-isolation three-dimensional rf component technologies that will enable complete system- or subsystem-level design and integration of rf and MMW systems will be presented. Advances in microfabrication techniques have enabled construction of air-core dielectric copper-based coaxial devices that form the building blocks for high-density high-connectivity subsystems and phased-array architectures.

4.2: A Ka-Band Dual-Polarized Flip-Chip TR-Cell MMIC Using 0.12-µm MHEMTs (3:50)

R. G. Freitag, D. M. Krafcsik, M. L. Salib, and K. M. Renaldo
Northrop Grumman ES, Baltimore, MD

A novel Ka-band flip-chip dual polarized TR-cell MMIC using 0.12-µm MHEMT technology will be described. Each polarization includes a 5-bit phase shifter, four-stage power amplifier, and a four-stage low-noise amplifier along with two SPDT switches for transmit/receive (T/R) signal separation. A 4-bit attenuator is common to both polarization paths. Overall transmit and receive gains between 15 and 20 dB were achieved across a 35–38-GHz band. TR cell yields, including both polarizations, greater than 30% were obtained.

4.3: Zero-Level Packaging for rf MEMS Switches (4:10)

D. Forehand and C. Goldsmith
MEMtronics Corp., Plano, TX

A zero-level packaging process (wafer-level micro-encapsulation) has been developed to effectively protect rf MEMS switches from harsh environments. This packaging technique is compatible with high-performance MEMS switches and demonstrated effective protection against humidity. The state of processing, rf measurements, and hermeticity testing of encapsulated rf MEMS packages will be updated.

4.4: Low-Temperature Wafer-Level Packaging for MMICs (4:30)

P. P. Chang-Chien, K. J. Tornquist, D. S. Farkas, and M. Nishimoto
Northrop Grumman Space Technology, Redondo Beach, CA

High-performance MMICs have been hermetically packaged by using a low-temperature wafer-level packaging process developed at NGST. Excellent performance from packaged MMIC circuits as well as from rf vias will be presented.

Session 5

ADVANCED ARRAY TECHNOLOGIES: SPACE AND GROUND APPLICATIONS

Tuesday, March 21 / 3:30 – 5:10 pm/ Room 2

Chair: **Christopher D. Lesniak**
Air Force Research Laboratory, Wright-Patterson AFB, OH

Co-Chair: **Bradley Paul**
Air Force Research Laboratory, Wright-Patterson AFB, OH

5.1: **RF on Flex Tile for L-Band Phased Arrays** **(3:30)**

A. Jacomb-Hood, E. Talley, E. Lier, and B. Acikel
LM CSS, Newtown, PA

5.2: **Air-Cooled Active Transmit/Receive Panel Array** **(3:50)**

A. Puzella and W. Payne
Raytheon, Sudbury, MA

G. Jerinic
Raytheon, Tewksbury, MA

A panel array to operate up to 20 W per channel using air or liquid cooling has been developed. Printed-wiring-board fabrication and automated assembly were utilized. The demonstration panel consists of 1024 CP radiators, RF power/logic distribution, and an embedded circulator layer. Measured active CP pattern, air-cooled performance will be presented.

5.2: **Flex-Based L-Band Phased-Array Antenna Demonstration** **(4:10)**

T. Dalrymple, C. Lesniak, P. Buxa, and R. Neidhard
AFRL/Sensors Directorate, WPAFB, OH

An L-band phased-array panel using rf-on-flex technology to minimize mass and cost has been fabricated and tested. The demonstration panel incorporated many novel technologies, including low-cost plastic packaging of MMIC die and light-weight flex-board materials. Control of the array was achieved through a low-cost FPGA controller and a Windows graphical user interface (GUI).

5.4: **Arrays of Random Sub-Arrays for Wideband Applications** **(4:30)**

K. C. Kerby and J. T. Bernhard
University of Illinois at Urbana-Champaign, Urbana, IL

Modifications to the geometry of random arrays, which improve manufacturability and the design process while preserving the characteristic wide pattern bandwidths of the random arrays, will be presented. Properties of these array factors were analyzed probabilistically and will be discussed.

5.5: LCP Package for Highly Integrated MMICs (4:50)

J. Dishong, R. Mongia, R. Thornton, and G. Clark
REMEC Defense & Space, Richardson, TX

A compact, multilayered, dc and 20 GHz, low-insertion-loss liquid-crystal-polymer (LCP) surface-mount quad flat no-lead (QFN) package has been developed for the AFRL for the packaging of highly integrated T/R MMICs, power amplifiers, and true-time-delay circuits.

Session 6

EMBEDDED C2

Tuesday / March 21 / 3:30 – 5:00 pm / Room 3

Chair: **Kathleen A. Griggs**
Puritan Research Corp., Vienna, VA

Co-Chair: **George F. Hurlburt**
Naval Air Warfare Center, Patuxent River, MD

6.1: Embedded Sensors in Macro Capabilities (3:30)

G. Hurlburt
Naval Air Warfare Center, Patuxent River, MD

The challenge of interoperability among DoD systems grows daily as systems of systems begin to comprise capabilities. The Global Information Grid (GIG) and its Net-Centric Enterprise Services (NCES) have immense command-and-control implications. All of this has a direct bearing on embedded sensor systems and extend into the micro-world. A firm understanding of agent-based software and its interaction with systems of systems is vital to future warfare.

6.2: Networked Embedded Systems Technology (3:50)

J. Paul
DARPA, Arlington, VA

The goal of NEST is to build dependable real-time distributed embedded applications. NEST is developing a repository of application-independent, customizable, and adaptable services for real-time coordination and synthesis of networked-embedded systems and integrating those services into military-focused ad-hoc wireless sensor network applications.

6.3: Weapons-Effects Assessment via Embedded Sensors (4:10)

K. J. Smart
Sandia National Laboratories, Albuquerque, NM

The recent Weapon-Effects Assessment via Embedded Sensors (WEAVES) DARPA seedling has studied the possibility of embedding sensors in explosive ordnance for monitoring strike effectiveness. Additionally, communications during the penetration event is also desired by WEAVES for real-time reporting of weapon trajectory. There are many required devices to make such a capability possible.

6.4: Military Relevance of Wireless Ad-Hoc Network Microsensors (4:30)

T. D. Cole and W. Bain
Northrop Grumman TASC, Tampa, FL

The results from numerous field assessments to underscore issues associated with large-scale (>100 nodes) operation of mote fields for DoD applications, in particular, the limitations observed with passive sensor modalities employed to date, will be presented. Opposing design forces and the integration/design rules that limit the utility of commercially available microsensors will be discussed. Finally, a technology solution that relies on active sensing modalities at the mote level will be described.

WEDNESDAY, 22 MARCH

Session 7

RAD-HARD BY DESIGN

Wednesday, March 22 / 8:30 – 10:10 am / Room 1

Chair: **Creigh Gordon**
AFRL/VSSE, Kirtland AFB, NM

Co-Chair: **John Franco**
Defense Threat Reduction Agency, Ft. Belvoir, VA

7.1: **Boeing–DARPA Rad-Hard–by–Design Program Results** **(8:30)**

Z. Johnson, W. Snapp, D. Chaney, and M. Baze
The Boeing Company. Seattle, WA

The results of the DARPA Rad-Hard–by–Design program that has demonstrated and characterized hardening techniques in advanced mixed-signal CMOS and SiGe processes from the trusted foundry will be reported. Hardening to strategic levels with acceptable area, power, and performance penalties will be described.

7.2: **Rad-Hard Technology Considerations for Space Systems** **(8:50)**

S. Doyle
BAE Systems, Manassas, VA

As commercial semiconductor technologies rapidly progress to 90 nm, 65 nm, and beyond, challenges, issues, and limitations will likely develop regarding suitability for space. Single-event-upset (SEU) hardening, parasitic effects, leakage currents, transients, and V_t/power-supply noise-rejection ratio are some of the issues that must be addressed.

7.3: **Investigation of the 130-nm Technology Node** **(9:10)**

K. Avery
ATK Mission Research, Albuquerque, New Mexico

Data will be presented for the work being done on the 130-nm technology node at ATKMR, in conjunction with its government partners AFRL, DARPA, and DTRA. The test chips were developed for bulk and SiGe processes, and the radiation and reliability characteristics will be examined.

7.4: **Next-Generation 16-Mbit Rad-Hard–by–design SRAM for Military Space Applications** **(9:30)**

C. Hafer, J. Mabra, D, Slocum, and A. Jordan
Aeroflex Colorado Springs, Colorado Springs, CO

A next-generation 16-Mbit asynchronous Rad-Hard–by–Design SRAM has been designed, manufactured, and radiation tested. State-of-the-art Rad-Hard–by–Design methodology has been advanced by embedding EDAC into the SRAM device along with using more-conventional Rad-Hard–by–Design techniques for the remaining device circuitry. Hardness results will be presented.

7.5: Hardness-by-Design: Current Status and Future Challenges (9:50)

R. C. Lacoe
The Aerospace Corp., Los Angeles, CA

Over the last decade, the idea that rad-hard components could be fabricated at commercial foundries using only design approaches to mitigate radiation effects has gone from the unthinkable to gaining a large degree of acceptance. The current status of this approach, referred to as hardness-by-design (HBD), will be summarized. In addition, future challenges facing HBD will be discussed, including HBD on commercial SOI and reliability and qualification issues.

BREAK (10:10–10:30)

Session 8

ADVANCED LINEARIZATION HIGH-EFFICIENCY POWER AMPLIFIERS

Wednesday, March 22 / 8:30 – 10:00 am / Room 2

Chair: **Chris W. Hicks**
Naval Air Systems Command, Patuxent River, MD

Co-Chair: **Peter M. Asbeck**
University of California San Diego, La Jolla, CA

8.1: Linear Response in Digital Amplifiers for Communications (8:30)

D. L. Miller, C. Lavoie, and J. X. Przybysz
Northrop Grumman Corp., Baltimore, MD

Switching amplifiers, when combined with an output filter, are being used as efficient amplifiers for audio systems. The extension to rf frequencies offers significant advantages to communications systems in terms of linear response and efficiency. The efforts toward development of a 225–400-MHz amplifier will be described.

8.2: Linearization and Memory Effect in High-Efficiency Envelope-Tracking GaN Power Amplifiers for Communications Applications (8:50)

P. Asbeck, D. Kimball, and J. Jeong
University of California San Diego, La Jolla, CA

P. Draxler
University of California San Diego, La Jolla, CA and Qualcomm, La Jolla, CA

A GaN-based power amplifier which attains 50% average power-added efficiency for WCDMA signals with 7.7-dB peak-to-average power ratio is described. The output power level is 37 W average and 220 W peak. Adaptive digital techniques were used for predistortion and correction of memory effect, resulting in an EVM below 1% and ACPR below –52 dBc.

8.3: Wide-Band Linearized GaN Power Amplifier (9:10)

A. Katz and M. Kubak
Linearizer Technology, Inc., Hamilton, NJ

An ultra-wide-band linearizer operating over the frequency range of 6–18 GHz, designed to work with a wide-band GaN power amplifier, will be described. A balanced architecture was used for both the amplifier and the linearizer to minimize harmonic distortion. The linearizer technology's unique active FET non-linear generator circuitry was used to correct harmonics. Linearizer HPA performance results will be presented. Correction was achieved across the entire band.

8.4: RF Power-Efficiency Improvement by Using Linearized SiGe Class-E Power Amplifiers for Joint Tactical Radio System Applications **(9:30)**

J. D. Popp
SPAWAR Systems Center San Diego, San Diego, CA

D. Y. C. Lie
Dynamics Research Corp., San Diego, CA

F. Wang and D. Kimball
University of California San Diego, San Diego, CA

A novel wide-band envelope-tracking technique to linearize RFIC SiGe Class-E power amplifiers for JTRS applications will be reported. Linearized power-amplifier performance for non-constant envelope signals, such as the JTRS OFDM signal, showing improved PAE while meeting spectral masks will be demonstrated.

BREAK **(10:00–10:30)**

Session 9

ELECTRONIC AND PHOTONIC ICs

Wednesday, March 22 / 8:30 – 10:00 am / Room 3

Chair: **Jagdeep Shah**
DARPA/MTO, Arlington, VA

Co-Chair: **Richard A. Soref**
Air Force Research Laboratory, Hanscom AFB, MA

9.1: **DARPA EPIC Program Update: Luxtera's Development of a 100-GB Transceiver Using CMOS Photonics Technology** **(8:30)**

C. Gunn
Luxtera, Carlsbad, CA

Through DARPA's EPIC Program, Luxtera has integrated a 100-GB optical transceiver into a production CMOS process. The transceiver integrates optical WDM filters, silicon modulators, and photodetectors alongside all required circuitry. The resulting 100-GB transceiver replaces racks of equipment with a single silicon die. Substantial cost and performance benefits are realized.

9.2: **Recent Advances in CMOS-Compatible Integrated Photonics** **(8:50)**

M. Grove, A. Pomerene, and T. Conway
BAE Systems, Manassas, VA

D. Carothers
BAE Systems, Nashua NH

D. M. Gill, M. S. Rasras, K-Y. Tu, S. S. Patel, Y-K. Chen, and A. E. White
Lucent Technologies, Murray Hill, NJ

L. C. Kimerling, J. Michel, M. Beals, and D. Sparacin
MIT, Cambridge, MA

BAE Systems, Lucent Technologies, Massachusetts Institute of Technology, and Applied Wave Research are participating in a high-payoff research and development program for the Microsystems Technology Office (MTO) of DARPA. Innovative approaches to materials development and device integration based on CMOS technology and CMOS-compatible photonic devices will be used to achieve a level of integration and increased performance unavailable by any other means. The goal of the program is the development of technologies and design tools necessary to fabricate an application-specific electronic photonic integrated circuit (AS-EPIC).

9.3: **Gigahertz High-Resolution Optical Sampling Technology (GHOST)** **(9:10)**

G. Barbastathis, J. Hoyt, E. P. Ippen, F. X. Kärtner, and M. Perrott
MIT, Cambridge, Massachusetts

The DARPA EPIC-GHOST Program at MIT is a coordinated effort by MIT Campus and MIT Lincoln Laboratory to demonstrate advanced photonic devices and interface circuits that can be integrated with silicon electronics for future high-performance computing and signal-processing applications. An overview on the current status of the program will be given.

9.4: SOI with Er:SiO_x Overcladding: Microphotonic Design and Fabrication for Ultra-Compact Amplifier Circuits and Low-threshold Broadband Si-Based Lasers (9:30)

O. Painter
California Institute of Technology, Pasadena, CA

A novel hybrid SOI/Er:SiOx chip technology for ultra-compact amplifying optical circuits and low-threshold broadband Si-based lasers is proposed. The optical design of such a microphotonic system will be presented, along with recent work on reducing on-chip optical loss and creating high-Q microdisk resonant cavities for Si-based lasers.

BREAK (10:00–10:30)

Session 10

RAD-HARD MICROELECTRONICS ROADMAPS (GOVERNMENT)

Wednesday, March 22 / 10:30 am – 12:10 pm / Room 1

Chair: **John Franco**
DTRA/TDAR, Alexandria, VA

Co-Chair: **Creigh Gordon**
AFRL/VSSE, Kirtland AFB, NM

10.1: **Overview Radiation-Hardened Electronics Oversight Council (RHOC)** **(10:30)**

C. Byvik and L. Palkuti
DTRA, Alexandria, Virginia

Ensuring that key government systems perform in expected radiation environments requires that DoD have sources of rad-hard microelectronics for which little commercial demand exists. The "corporate" manner in which the RHOC develops one roadmap with milestones, funding, and management assignments to meet Program Office technology freeze dates will be discussed.

10.2: **Defense Threat Reduction Agency Rad-Hard Microelectronics Program: Past, Present, and Future** **(10:50)**

J. Franco, L. Cohn, A. Clark, and L. Palkuti
Defense Threat Reduction Agency, Alexandria, VA

The background, mission, objectives, technical investment strategy, and technology roadmap of the Defense Threat Reduction Agency (DTRA) Radiation-Hardened Microelectronics (RHM) Program will be discussed. This program operates in coordination with various other DoD and government organizations, through the guidance of the Deputy Director for Research and Engineering (DDR&E) Radiation-Hardened Microelectronics Oversight Council (RHOC), to ensure the availability of hardened microelectronics and other technologies to support the needs of DoD missions with nuclear hardening and survivability requirements.

10.3: **The NASA Electronic Parts and Packaging (NEPP) Program: Roadmap for NASA's Radiation Effects on and Reliability of Electronics Efforts** **(11:10)**

K. A. LaBel and M. J. Sampson
NASA/GSFC, Greenbelt, MD

The NEPP Program is responsible for developing the plans for and leading the research on reliability and radiation response in the space and aeronautics environments. The updated NASA task list as well as a consideration of future research areas will be presented.

10.4: Sandia National Laboratories' Microelectronics Program **(11:30)**

K. K. Ma and P. E. Dodd
Sandia National Laboratories, Albuquerque, NM

Sandia National Laboratories plays a major role in advancing microsystems research and development and in incorporating microsystems into the nuclear stockpile. An overview of the Sandia's Rad-Hard Microelectronics Program and the role of Sandia's Microsystems and Engineering Sciences and Applications complex in shaping the future of rad-hard microelectronics will be presented.

10.5: Spacecraft Microelectronics: Roadmap for a Pervasive Technology Base at the Air Force Research Laboratory **(11:50)**

C. Gordon
AFRL/VSSE, Kirtland AFB, NM

In support of a military strategy based on information superiority, the Air Force Research Laboratory's Space Vehicles Directorate is forwarding a pervasive spacecraft microelectronics technology base. Programs are mapped into electronic foundations, components, microsystems, and protection groups.

LUNCH **(12:10–1:30)**

Session 11

RF POWER

Wednesday, March 22 / 10:30 am – 12:00 pm / Room 2

Chair: **Steven C. Binari**
Naval Research Laboratory, Washington, DC

Co-Chair: **Gerald M. Borsuk**
Naval Research Laboratory, Washington, DC

11.1: High-Power S-Band and X-Band Wide-Bandwidth GaN MMICs **(10:30)**

D. Partlow, M. Aumer, H. Henry, and B. Veasel
Northrop Grumman Corp., Baltimore, MD

High-performance GaN power HFETs have been developed for MMICs with high power at S-band. In addition, 2–18-GHz wide-bandwidth MMICs have been developed for system applications. Northrop Grumman's GaN MMIC technology, including SiC substrate readiness, state-of-the-art film growth, circuit design, fabrication, and power testing, will be discussed.

11.2: Affordable High-Power AlGaN/GaN HEMTs on 4-in. 3C Poly-SiC Substrates **(10:50)**

G. Augustine, J. D. Hartman, and E. C Elvey
Northrop Grumman Corp., Baltimore, MD

E. L. Piner
Nitronex Corp., Raleigh, NC

The fabrication of AlGaN/GaN HEMTs grown on thin-film <111> silicon bonded to 4-in. 3C polycrystalline-SiC substrate will be reported. This fabrication method takes advantage of the high thermal conductivity, large diameter, and low cost of poly-SiC substrates. At 2.14 GHz and 15 V, the output power was 24.7 dBm with a gain of 15.4 dB and a PAE of 60%

11.3: High-Power AlGaN/GaN HEMTs for Millimeter-Wave Applications **(11:10)**

T. Palacios, A. Chakraborty, S. Keller, and S. P. DenBaars
University of California at Santa Barbara, Santa Barbara, CA

Recent progress on AlGaN/GaN HEMTs for power amplification at Ka-band will be reviewed. The combination of novel HEMT structures with advanced processing has allowed the fabrication of transistors with record small-signal performance, as well as more than 10 W/mm of output power at 40 GHz.

11.4: On-Wafer High-Resolution Phase-Noise Measurements and the Detection of Traps in GaAs **(11:30)**

D. E. Dawson, A. Ezis, and B. S. Hewitt
Northrop Grumman Corp., Baltimore, MD

Traps at baseband in GaAs MMICs produce unwanted side bands on an rf carrier. Screening wafers for this problem in order to meet system specs in final test is recommended. Singling out low-level side bands due to traps requires spurious-free low-phase-noise measurement techniques. These techniques as applied to on-wafer measurements suitable for screening wafers are described.

LUNCH **(12:00–1:30)**

Session 12

HIGH-PERFORMANCE LOW-NRE ELECTRONICS

Wednesday, March 22 / 10:30 am – 12:00 pm / Room 3

Chair: **Daniel J Radack**
DARPA, Arlington, VA

12.1: Asynchronous Logic Design for Rad-Hard Structured ASICs **(10:30)**

J. Teifel, R. S. Flores, and K. K. Ma
Sandia National Laboratories, Albuquerque, NM

Asynchronous logic provides lower power, reduced electromagnetic emissions, and greater robustness for high-consequence government applications. Emerging one-mask-structured ASIC architectures are well-suited for both asynchronous and more-conventional synchronous digital designs. An automated asynchronous design flow for a structured ASIC built in Sandia's rad-hard 0.35-µm SOI process will be discussed.

12.2: LSI Logic's MIL/Aero-Structured ASIC Approach: RapidChip **(10:50)**

J. P. Bendekovic
LSI Logic, Leesburg, VA

LSI Logic will discuss their RapidChip technology for military and aerospace digital logic. LSI Logic offers not only cell-based ASICs but also the RapidChip Platform, or "structured" ASICs, for quicker turn-around time and lower NRE costs. RapidChip also offers low power, SEU immunity, non-volatile logic, and design security.

12.3: Closing the ASIC-Design Productivity Gap **(11:10)**

R. Brees, S. Fischer, M. Carson, and T. Dao
Boeing Phantom Works, Seattle, WA

The cost of developing ICs to meet the demanding requirements of DoD systems is increasing rapidly. IC design tools have not kept pace with the capabilities of IC fabrication technologies. Boeing, under two DARPA programs (MSP and CLASS), is addressing this design productivity gap by increasing the performance of ASICs using design automation instead of custom techniques and by implementing clockless design techniques. The methodologies and benefits of these approaches will be discussed.

12.4: How to Get Low-Cost and High-Performance Electronics by Just Waiting Around **(11:30)**

B. S. Cohen, J. Jacob, and V. Sharma
Institute for Defense Analyses, Alexandria, VA

Direct approaches to reducing the NRE costs in obtaining state-of-the-art ICs have had limited success. A different approach is to alter system development and production strategies, deferring binding to hardware and employing virtual machines. This study looks at the impact these approaches can have for increasing the performance of microelectronics in deployed defense systems, while simultaneously reducing costs

LUNCH **(12:00–1:30)**

Session 13

RAD-HARDENED MICROELECTRONICS ROADMAPS (INDUSTRY)

Wednesday, March 22 / 1:30 – 3:00 pm / Room 1

Chair: **John Franco**
DTRA/TDAR, Alexandria, VA

Co-Chair: **Creigh Gordon**
AFRL/VSSE ,Kirtland AFB, NM

13.1: BAE Systems' Rad-Hard Microelectronics Technology and Product Roadmaps (1:30)

L. Rockett
BAE Systems, Manassas, VA

BAE Systems, in partnership with the DoD under the Rad-Hard Microelectronics Accelerated Technology Development Initiative, has completed the modernization of its microelectronic process facility located in Manassas, Virginia. The foundry is now in full production at the rad-hard 250- and 150-nm technology nodes, supporting a large portfolio of products and services to meet DoD program requirements through 2012 and beyond. The details will be provided.

13.2: Honeywell Microelectronics' Technology Development Program (1:45)

R. R. Katti, R. J. Scheulke, T. J. Romanko, G. S. Panning, D.C. Anthony, R. L. Clark, and H. N. Kaakani
Honeywell, Inc., Plymouth, MN

Deep submicron silicon-on-insulator (SOI) technology advancements at Honeywell have enabled new generations of low-power high-performance products. Current efforts on 0.35-μm and 150-nm SOI technologies, advanced ASICs, 16M SRAM products, non-volatile memory, and mixed-signal technologies will be described.

13.3: Low-Volume Fabrication Access to Commercial Foundry: Jazz Semiconductor Technology's Roadmap (2:00)

R. Van Art
Jazz Semiconductor, Newport Beach, CA

Jazz Semiconductor will examine the role of pure play specialty foundries within the rad-hard community. Particularly, hurdles essential to overcome if seamless support of HBD and HBP approaches are to be adopted will be addressed. A technology roadmap will be presented.

13.4: Rad-Hard Non-Volatile Reprogrammable FPGAs: Actel Corp.'s Roadmap (2:15)

B. Cronquist, T. Farinaro, K. O'Neill, and R. Pragsam
Actel Corp., Mountain View, CA

Actel Corp.'s roadmap of hardened FPGA offerings will be described. Both the non-volatile one-time programmable (OTP) FPGA and the non-volatile re-programmable FPGA roadmap will be discussed. Commercial, MIL-temp, rad-tolerant, and rad-hard-specific efforts will be described. Special attention will be given to the definition, technical challenges, and mitigations for the radiation-tolerant non-volatile reprogrammable FPGA at advanced process nodes (90 nm and below).

13.5: Boeing's Rad-Hard Microelectronics Design Technology Roadmap **(2:30)**

W. P. Snapp and Z. Johnson
The Boeing Company, Seattle, WA

Boeing's roadmap for development of rad-hard microelectronics design capability and applications which drive its requirements will be described. The roadmap features development of mixed-signal libraries and integrated EDA, both for hardened and non-hardened commercial fabrication processes based on innovative foundry flexible synthesis techniques.

13.6: Radiation-Effects Modeling Roadmap for Emerging Technologies **(2:45)**

L. W. Massengill, R. D. Schrimpf, R. A. Weller, and R. L. Reed
Vanderbilt University, Nashville, TN

An overview of radiation-effects modeling activities at the Vanderbilt Institute for Space and Defense Electronics will be presented. Emerging issues, including nanometer scaling and advances in computational CAD capabilities, that impact the simulation and prediction of IC radiation response in space and weapon environments will be cited. An integrated modeling roadmap for radiation-effects analysis in advanced technologies will be presented.

BREAK **(3:00–3:30)**

Session 14

POWER ELECTRONICS I

Wednesday, March 22 / 1:30 – 3:00 pm / Room 2

Chair: **Fritz Kub**
Naval Research Laboratory, Washington, DC

Co-Chair: **Gerald M. Borsuk**
Naval Research Laboratory, Washington, DC

14.1: SiC: The Future of High-Power Electronics **(1:30)**

S. Beermann-Curtin
Defense Advanced Research Projects Agency, Arlington, VA

The current status of the SiC materials and components emphasizing the work through the WBST-HPE program will be discussed. The SSPS development and EMALS, and an insertion plan into aircraft carriers, will be described.

14.2: Silicon Carbide Devices for High-Power Applications **(1:50)**

J. Palmour
Cree, Inc., Durham, NC

Silicon Carbide (SiC) power devices offer tremendous potential over existing silicon power devices due to the much higher breakdown electric field in SiC. The first devices being manufactured in volume are SiC Schottky diodes, which are replacing ultra-fast Si PiN diodes in switch-mode power supplies and are emerging in applications in motor controls and hybrid electric vehicles. The ever improving crystal quality of the 3-in.-diameter 4H-SiC substrates has allowed excellent yields and reliability, enabling SiC to finally start to displace silicon. More importantly, recent efforts on 100-mm diameter wafers have yielded exciting results. A detailed review of the current state of the art in SiC material and large-area power devices will be provided.

14.3: High-Power-Density Components for Power Switching and Conditioning Applications **(2:10)**

C. J. Scozzie, C. W. Tipton, D. Katsis, and B. Geil
Army Research Laboratory, Adelphi, MD

The stringent mass and volume requirements for future hybrid electric military power systems provide a mandate to investigate high-power-density components that will provide the most-compact power conversion and distribution systems possible. The state of the art in power density for power components will be discussed.

14.4: Silicon Carbide VJFETs for High-Frequency Cascode Circuits in Power-Conversion Applications **(2:30)**

C. J. Scozzie, C. W. Tipton, D. Katsis, and B. Geil
Army Research Laboratory, Adelphi, MD

S. Van Campen, V. Veliadis, T. McNutt, and E. Stewart
Northrop Grumman, Linthicum, MD

A new normally off 4H-SiC cascode circuit has been developed, offering a low-specific on-resistance and over 1000-V blocking capability. A low-voltage normally off SiC JFET was used as the controlling device in series with a high-voltage normally on SiC JFET capable of blocking over 1000 V.

BREAK **(3:00–3:30)**

Session 15

HIGH-PERFORMANCE INTEGRATED ELECTRONICS I

Wednesday, March 22 / 1:30 – 3:00 pm / Room 3

Chair: **Mark Rosker**
DARPA/MTO Arlington, VA

Co-Chair: **Cynthia Hansen**
SPAWAR Systems Center, San Diego, CA

15.1: Efficient Antimonide-Based Compound Semiconductor MMICs **(1:30)**

B. Brar, J. Bergman, J. Hacker, and G. Sullivan
Rockwell Scientific, Thousand Oaks, CA

Antimonide-based compound semiconductor (ABCS) materials, process, devices, and circuits for high-performance low-dissipated-power technology will be discussed. The performance of superior low-power and low-noise operation of MMICs using ABCS transistors will be described.

15.2: Antimonide-Based Compound Semiconductors (ABCS) Technology for High-Speed Low-Power Electronics **(1:50)**

A. Gutierrez-Aitken, R. Tsai, C. Monier, and W. Deal
Northrop Grumman Space Technology, Redondo Beach, CA

Northrop Grumman Space Technology has developed narrow-bandgap microelectronics under the Antimonide-Based Compound Semiconductors DARPA program. In this effort, state-of-the-art high-electron-mobility transistors (HEMTs) and heterojunction bipolar transistor (HBT) technologies were developed for ultra-low-power low-noise amplifiers, and low-power high-speed digital and mixed-signal applications.

15.3: Antimonide-Based Compound Semiconductors (ABCS) Technology for High-Speed Low-Power Mixed-Signal and Front-End Electronics **(2:10)**

K. Elliott
HRL Laboratories, LLC, Malibu, CA

HRL Laboratories has developed transistors and integrated circuits with state-of-the-art power delay based on InAs and related materials. HBT-based circuits exhibit f_t > 200 and f_{max} > 126 GHz and HEMT devices exhibit f_t > 300 GHz. Such devices will enable a new class of applications with very low power consumption at microwave and millimeter-wave operating frequencies.

15.4: Ultra-Fast SiGe HBT Technology: Today and and Tomorrow **(2:30)**

D. C. Ahlgren, M. Khater, T. Adam, and F. Pagette
IBM Corp., Hopewell Junction, NY

The final results from the Ultra-Fast SiGe HBT work supported by TEAM, will be presented, which simultaneously achieved an ac performance of f_t = 300 GHz with an f_{max} = 400 GHz, allowing the demonstration of a 3.2 psec/stage ring oscillator and noise figure (F_{min}) of 1.0 dB at 25 GHz. SiGe HBT development possibilities making 500 GHz possible will also be discussed.

BREAK **(3:00–3:30)**

Session 16

FIELD/CIRCUIT INTERACTION AND SIGNAL PROCESSING

Wednesday, March 22 / 3:30 – 5:00 pm / Room 1

Chair: **Michael B. Steer**
North Carolina State University, Raleigh, NC

Co-Chair: **Lawrence Carin**
Duke University, Durham, NC

16.1: Signal Processing and Sensor Management for Detection of Concealed Electronic Devices **(3:30)**

L. Carin
Duke University, Durham, NC

A partially observed Markov decision process (POMDP) is employed for the analysis of standoff rf sensing of electronic devices. The POMDP develops a policy to optimally employ sensor resources, based upon the data that has been observed. In addition to the POMDP, this problem is also addressed in the context of model free reinforcement learning.

16.2: Modeling and Characterization of the Intermodulation Response of a Remote Nonlinear System **(3:50)**

A. Walker, J. Wilkerson, K. Gard, and M. Steer
NC State University, Raleigh, NC

The intermodulation response can be used to extract the characteristics of a nonlinear system especially of one that must be probed remotely. Information is contained in the broadband amplitude and phase characteristics. Modeling of such as system and experimental means for characterizing the response will be reported.

16.3: fREEDA-Compatible Stamps for Semi-Discrete Forms of Maxwell's Equations **(4:10)**

A. Cangellaris and A. Ramachandran
University of Illinois, Urbana, IL

A methodology is proposed for the development of appropriate equivalent-circuit stamps for the direct incorporation of semi-discrete forms of Maxwell's curl equations in the general-purpose multi-physics nonlinear simulator fREEDA. The proposed stamps are also compatible with other SPICE-like transient non-linear circuit simulators.

16.4: Forensic Characterization of Circuits **(4:30)**

E. J. Delp and A. F. Martone
Purdue University, West Lafayette, IN

E. J. Delp and A. F. Martone
Purdue University, West Lafayette, IN

The methods for forensic characterization of rf circuits will be described. Forensic characterization is the ability to determine the circuit configuration by observing a return signal after the circuit has been probed with a particular rf signal. Circuits can be characterized based on the scattering physics that are produced when an external probe signal encounters nonlinear components in the circuit. Based on measurements of the rf signature, the circuit can be identified using statistical classification techniques.

Session 17

POWER ELECTRONICS II

Wednesday / March 22 / 3:30 - 5:00 pm / Room 2

Chair: **Fritz Kub**
Naval Research Laboratory, Washington, DC

Co-Chair: **Gerald M. Borsuk**
Naval Research Laboratory, Washington, DC

17.1: Wide-Bandgap Semiconductor Devices for Next-Generation Power Processing **(3:30)**

J. Tucker, L. Stevanovic, K. Matocha, and S. Arthur
General Electric GRC, Niskayuna, NY

Power devices built using wide-bandgap (WBG) semiconductor materials, such as SiC and GaN, offer significant performance advancements over their silicon counterparts, due to higher blocking-field capability, faster switching speed, and higher temperature (> 200°C) operation. These WBG devices will enable a new generation of power-processing systems. Applications include high-density power converters, where faster switching speeds enable the reduction of passive components and higher-temperature devices to reduce cooling requirements. WBG power devices will also enable advanced pulsed-power supplies for next-generation propulsion and directed-energy weapons.

17.2: A Comparison of SiC Power Switches for Hi-Rel Defense Applications **(3:50)**

J. B. Casady and M. S. Mazzola
SemiSouth Laboratories, Starkville, MS

Results from 600- and 800-V VJFETs switching up to 150 A, suitable for power supply and motor drive applications, will be presented along with optimized applications circuits emphasizing inherent safety with VJFET power switches.

17.3: Status of High-Voltage High-Frequency Silicon-Carbide Power Devices **(4:10)**

A. Hefner
NIST, Gaithersburg, MD

The emergence of high-voltage high-frequency (HV-HF) silicon carbide (SiC) power devices is expected to revolutionize utility and military power distribution and conversion systems. The DARPA Wide-Band-Gap (WBG) High-Power Electronics (HPE) program is spearheading the development of HV-HF SiC power semiconductor technology. Detailed characteristics of the HPE program devices will be presented and the circuit performance enabled by these devices will be discussed. The device characteristics presented include high-voltage blocking, static conduction, switching, safe-operating area, and reliability.

17.4: DC/DC Converters for Phased-Array Radar **(4:30)**

G. Skutt
VPT, Inc., Blacksburg, VA

A relatively high-power-density commercial-off-the-shelf (COTS) dc-dc module was developed for phased-array radar applications. The critical design criteria are 1-kW output, 90% efficiency, full-brick size, and flexibility for different radar systems. Converter cost, reliability, and qualification will also addressed.

Session 18

HIGH-PERFORMANCE INTEGRATED ELECTRONICS II

Wednesday, March 22 / 3:30 – 5:30 pm / Room 3

Chair: Daniel J. Radack
DARPA/MTO Arlington, VA

Co-Chair: Stephen A. Pappert
DARPA/MTO Arlington, VA

18.1: Mixed-Signal SiGe Radar-on-a-Chip **(3:30)**

M. Lucas, H. Ball, A. Turley, and C. Marcelli
Northrop Grumman Corp., Baltimore, MD

18.2: InP HBT Electronics for High-Performance Mixed-Signal Electronic-Warfare Applications **(3:50)**

M. Le
Vitesse Semiconductor, Camarillo, CA

F. Stroili, R. Elder, and J. Feng
BAE Systems, Nashua, NH

The development of a high-performance InP HBT technology, as well as the implementation of high-speed mixed-signal circuits including a high-frequency direct digital synthesizer and other related high-speed mixed-signal circuits will be reported. This work is being performed under the DARPA TFAST (Technology for Frequency Agile Digitally Synthesized Transmitters) program.

18.3: High-Speed InP HBT Microelectronics at Northrop Grumman Space Technology **(4:10)**

A. Gutierrez-Aitken, D. Sawdai, C. Monier, and P. Chang
NGST, Redondo Beach, CA

Northrop Grumman Space Technology is developing InP HBT microelectronics for next-generation high-performance aerospace and defense applications. The status of all of our InP HBT technologies, including production and advanced processes, device performance, technology readiness levels, reliability, radiation hardness, and circuit demonstrations, will be highlighted.

18.4: Multi-GHz Direct Digital Synthesis Using 0.25-µm InP HBT Technology **(4:30)**

K. Elliott, M. Sokolich, T. Hussain, and D. A. Hitko
HRL Laboratories, LLC, Malibu, CA

A 0.25-µm InP HBT-based direct digital synthesizers ICs with clock rates in excess of 12 GHz will be reported. These exhibit a Nyquist-limited SFDR of > –30 dBc while supporting output frequencies from 0.0 to approximately 5.5 GHz. The clock frequency/power consumption FOM for this chip is roughly 1.5 GHz/W.

18.5: Radio-Frequency CMOS for Ultra-Low-Power Applications (4:50)

S. Subbanna, R. Wachnik, J. Pekarik, and M. Hakey
IBM Corp., Hopewell Junction, NY

MOSFETs in leading-edge CMOS technology nodes exhibit an f_t in excess of 300 GHz. Using both classical FET scaling and process innovations in the most advanced generations, these FETs can offer usable gain at voltages well below 0.5 V. The feasibility of CMOS in ultra-low-voltage SOC applications will be explored.

18.6: Silicon-Germanium-Based Millimeter-Wave ICs for Gbps Wireless Communications and Radar Systems (5:10)

B. Gaucher
IBM T. J. Watson Research Center, Yorktown Heights, NY

A. Joseph and E. Mina
IBM Systems and Technology Group, Essex Junction, VT

R. Wachnik
IBM Systems and Technology Group, Hopewell Junction, NY

The viability and suitability of silicon germanium (SiGe8HP) technology, enablement tools, and circuits to millimeter-wave applications today and a roadmap to the future has been validated. Key elements to be discussed include SiGe technology and design enablement advancements leading to the world's most highly integrated, lowest-power 60-GHz transmitter/receiver ICs.

THURSDAY, 23 MARCH

Session 19

WIDE-BANDGAP SEMICONDUCTORS

Thursday, March 23 / 8:30 – 10:00 am / Room 1

Chair: **Mark Rosker**
DARPA/MTO, Arlington, VA

Co-Chair: **Chris Bozada**
AFRL/SND, Wright-Patterson AFB, OH

19.1: GaN HEMT Technology for Q-band Power Amplifiers **(8:30)**

The progress made on the DARPA WBGS-RF Q-band Track program will be discussed. A 40-GHz device performance of simultaneous 7.3-dB gain, 3.3-W/mm output power, and 33% power-added efficiency from 500-µm total gate periphery HEMT devices has been demonstrated.

M. Wojtowicz, R. Coffie, I. Smorchkova, and B. Heying
Northrop Grumman, Redondo Beach, CA

19.2: Gallium Nitride Development for Wide-Band Applications **(8:50)**

A. Balistreri, P. Saunier, and C. Lee
TriQuint Semiconductor, Richardson, TX

P. C. Chao
BAE Systems, Nashua, NH

TriQuint Semiconductor and its partners, BAE Systems, Lockheed Martin, Emcore, II-VI, and Nitronex, are developing gallium nitride devices suitable for wide-band applications. The goals of the program are to produce reliable, reproducible high-performance devices and demonstrate capabilities through a 100-W 2–20-GHz module. The program encompasses continued improvement in material capabilities, development of device structures and process techniques, design and fabrication of MMICs, and thermal and mechanical design of high-power combiners and modules. The team will report on its progress and technical approach.

19.3: Raytheon–Cree Team DARPA WBGS Phase 2 Program Status **(9:10)**

J. Smolko
Raytheon Co., Tewksbury, MA

J. Milligan
Cree, Inc, Durham, NC

The Raytheon-Cree WBGS is accelerating the pace of GaN technology development to align with military and commercial system needs and to reduce insertion risk. Close coordination and open sharing between the two foundries eliminates duplication of development effort and reduces risk against technical hurdles. Progress on the WBGS program since its inception will be presented.

19.4: DARPA Wide-Band-Gap Semiconductors for rf Applications (WBGS-RF) Tri-Service Reliability Testing **(9:30)**

S. C. Binari and J. Roussos
Naval Research Laboratory, Washington, DC

G. D. Via
Air Force Research Laboratory, Dayton, OH

E. Viveiros
Army Research Laboratory, Adelphi, MD

The Tri-Service Team will present reliability data taken in support of DARPA's Wide-Band-Gap Semiconductors for rf Applications (WBGS-RF) program. Testing methodology and flow will be described. In addition, thermal modeling of unit cells along with Raman junction temperature (T_j) data will be shown.

BREAK **(10:00–10:30)**

Session 20

TRUSTED ELECTRONICS I

Thursday, March 23 / 8:30 – 10:00 am / Room 2

Chair: **E. D. (Sonny) Maynard**
ODUSD(S&T), Washington, DC

Co-Chair: **Ray A. Price**
Department of Defense, Fort George G. Meade, MD

20.1: Defense Trusted Integrated Circuit Policy **(8:30)**

E. D. (Sonny) Maynard
ODUSD(S&T), Washington, DC

Defense integrated circuits are obtained from global sources, which may expose defense systems to exploitation. Practices and policies now require that defense-acquisition programs actively manage their IC supply chains, anticipate potential threats posed by outsourcing practices, formally assess their system's vulnerabilities, and employ trusted suppliers and/or risk mitigation.

20.2: Obtaining Defense Access to Fabrication **(8:40)**

D. Radack
DARPA/MTO, Arlington, VA

Affordable access to leading-edge semiconductor technologies for research and prototyping has been a challenge to DoD for many years. Multi-Project Wafers (MPWs) are a promising solution for defense applications which need low volumes of advanced IC technologies. The experience of producing MPWs through the Trusted Foundry and the role of MPWs for DoD applications will be summarized.

20.3: DARPA Trust Program **(8:50)**

D. Collins
DARPA/MTO, Arlington, VA

Ensuring that ICs (or hardware and software in general) can be trusted to operate as intended is a very difficult problem. DARPA is exploring research and technology that can ensure that ICs operate as intended (no more, no less) despite being manufactured, packaged, or even operated by potential adversaries.

20.4: Trusted Microelectronics Hardware **(9:10)**

C. Ristich
AFRL/SNT, Wright-Patterson AFCB, OH

The potential vulnerabilities and mitigation techniques for ICs based on advanced hardware designs and anti-tamper (AT) technologies will be discussed. Hardware vulnerabilities and AT techniques are established through a compilation of recent open-source technical papers. Both invasive and non-invasive reverse engineering attacks will be addressed.

20.5: IBM's 90-nm Technology and Enablement (9:30)

M. Kerbaugh
IBM Systems and Technology Group, Essex Junction, VA

90-nm technology is the exciting new technology being offered through IBM's Trusted Foundry relationship with the U.S. Government. IBM's 90-nm technology and enablement, including manufacturing, ASIC design system, and foundry enablement, will be described. The technology including device, back end of line dielectrics, and wiring capabilities in both a performance-oriented technology and also in a low-power analog-oriented offering will be described. Yields and manufacturing performance relative to ITRS roadmaps will be updated. In the performance-oriented technology, IBM's ASIC design system at 90-nm, elaborating on some of the internal tools being developed, the supported IP, and the ASIC engagement model, will be discussed. Following an introduction to the Foundry Engagement model, the ASIC verses Foundry methodologies for the performance offering will be compared and contrasted. Details of the Foundry offering for both the performance-oriented technology as well as the low-power analog technology will be discussed, including library, IP, and reference flow support.

BREAK (10:00–10:30)

Session 21

SPACE APPLICATIONS I

Thursday, March 23 / 8:30 – 9:50 am / Room 3

Chair: **Charles Barnes**
NASA Jet Propulsion Laboratory, Pasadena, CA

Co-Chair: **Ken Hunt**
Air Force Research Laboratory, Kirtland AFB, NM

21.1: **Phase-Comparison Digital Tracker for Retrodirective Phased Array** **(8:30)**

J. Lux, A. Boas, S. Li, and R. McMaster
Jet Propulsion Laboratory, Pasadena, CA

Analysis and experimental results will be presented for a novel hybrid analog/digital system measuring the received phases of an incident 7.1-GHz signal in a four-element 1.8-m array. The measurements are used to form a retrodirective beam, independently of mechanical or electrical changes.

21.2: **Fault-Tolerant Power-System Architecture** **(8:50)**

S. Dawson, V. Moreno, G. Carr, and G. Wester
Jet Propulsion Laboratory, Pasadena, CA

A fault-tolerant power-system architecture can be implemented by using rad-hard mixed-signal ASICs. As the power demand increases for the future missions, simple block-redundant power-system architectures would penalize the system-level resources. A single fault-tolerant power system does not necessarily meet the overall reliability requirement of the mission. Depending on the power level, the power system could contain enough complexity that would require the fault of the containment regions to be reduced in order to maintain enough reliability in the mission. In order to reduce the fault containment regions, an architecture must be implemented that can provide communication among the functional elements as well as fault isolation.

21.3: **CMOS Active Pixel Sensor Technology and Reliability Characterization Methodology** **(9:10)**

Y. Chen, S. Guertin, B. Pain, and S. Kayali
Jet Propulsion Laboratory, Pasadena, CA

A JPL-designed 512 × 512 CMOS active pixel imaging system and the qualification methodology and reliability analysis approach for imaging sensors will be described. Both overall sensor reliability and pixel reliability will be presented.

21.4: The Growing, Critical Need for Reliable Non-Volatile Memory for Space Applications **(9:30)**

K. Hunt
Air Force Research Laboratory, Kirtland AFB, NM

J. Marshall
BAE Systems, Manassas, VA

While a reliable, dense, affordable non-volatile memory has always been a significant system design issue for space applications, the increased use of SRAM-based field-programmable gate arrays in space has made the problem far greater. The role of non-volatile memory in volatile FPGAs will be discussed and an approach to provide a space-qualifiable solution described.

BREAK **(9:50–10:30)**

Session 22

VERTICALLY INTERCONNECTED SENSOR ARRAYS

Thursday, March 23 / 10:30 am – 12:00 pm / Room 1

Chair: **Ray Balcerak**
DARPA/MTO, Arlington, VA

Co-Chair: **Dorota Temple**
RTI International, Research Triangle Park, NC

22.1: **3-D Integration Technology Platform for High-Performance Detector Arrays** **(10:30)**

D. Temple
RTI International, Research Triangle Park, NC

C. A. Bower, D. Malta, and J.E. Robinson
DRS Infrared Technologies, Dallas, TX

A platform technology for three-dimensional (3-D) integration of detector layers with multiple layers of silicon ICs to dramatically enhance on-chip signal-processing capabilities of the detector will be described. The implementation of the platform technology in high-resolution IR staring focal-plane-array (FPA) devices will be discussed.

22.2: **Vertically Integrated Sensor Arrays (VISA) for Enhanced-Performance HgCdTe FPAs** **(10:50)**

D. Temple, D. Malto, and C. Bower
RTI international, Research Triangle Park, NC

J. Robinson, L. Wood, E. Krueger, P. Coffman
DRS Infrared Technologies, Dallas, TX

HgCdTe focal-plane arrays (FPAs) offer the ultimate in IR sensitivity and find application in high-performance military systems. VISA technology is in development to achieve even higher-performance levels by providing increased signal processing at the pixel level. Performance data from VISA circuits as well as FPA data taken from VISA test structures will be discussed.

22.3: **InGaAs Focal-Plane Arrays for Low-Light-Level Visible and Short-Wave IR Imaging** **(11:10)**

B. M. Onat, R. M. Brubaker, M. Lin, and M. A. Blessinger
Sensors Unlimited, Inc., Princeton, NJ

Recent technological advances in detector design, epitaxial growth, processing, and readout IC design enabling extremely low-light level imaging throughout the visible and short-wave IR bands will be reported. These imagers enable a full day/night-imaging capability and at the same time are responsive to currently fielded laser designators, illuminators, and range finders.

22.4: Advances in Ultra-Sensitive SWIR Arrays for Low-Light-Level Imaging **(11:30)**

A. Hoffman, J. Rosbeck, D. Acton, and M. Jack
Raytheon Vision Systems, Goleta, CA

Large focal planes with InGaAs or HgCdTe detector arrays have been developed that meet the demanding requirements of astronomy and other low-background systems. With high quantum efficiency between 0.9 and 1.7 μm, these detectors are ideally suited for many SWIR applications. The design and performance of an ultrasensitve imaging array with more than one million detector pixels (1280 × 1024 elements) will be described. This imaging array was developed by Raytheon in support of DARPA's MANTIS program. Recent field data will be presented, and continuing advances in the development of ultrahigh-sensitivity SWIR imagers will be discussed.

LUNCH **(12:00–1:30)**

Session 23

TRUSTED ELECTRONICS II

Thursday, March 23 / 10:30 am – 12:00 pm / Room 2

Chair: **E. D. (Sonny) Maynard**
ODUSD(S&T), Washington, DC

Co-Chair: **Ray A. Price**
Department of Defense, Fort George G. Meade, MD

23.1: **The MPW Process: Understanding the Recipe for Success on Silicon** **(10:30)**

J. Meinhardt
Honeywell FM&T, Kansas City, MO

C. Turner
Insyte Corp., St Petersburg, FL

The Multi Project Wafer business model encompasses a complex series of tasks required to deliver end product to customers. An understanding of the required deliverables reduces potential silicon errors and shortens the wafer delivery cycle.

23.2: **A Non-Volatile Memory Technology for Tomorrow's Electronic Systems** **(10:50)**

C. Ng
Kilopass, Santa Clara, CA

Increased data and software IP security, expanding non-volatile storage, and lower cost are some of the challenges faced by evolving electronic systems. A highly secure, high-reliability, embedded non-volatile memory technology that requires only a standard logic CMOS process and is scalable to 90 nm and future process nodes will be described.

23.3: **A User's Perspective on the Application of the DoD Trusted Foundry Program** **(11:10)**

C. D. Caposell
Naval Air Systems Command, Aircraft Division, Patuxent River, MD

G. Walters
CPU Technology, Inc., Reston, VA

The Department of Defense recently initiated the Trusted Foundry Program to address the need for an assured supply of trusted microelectronic components for critical defense applications. Our experience with the Trusted Foundry contractor, IBM, lessons learned, future plans for the Trusted Foundry, and recommendations for process improvements will be discussed.

23.4: The Trusted Foundry Fabrication of a New Class of "System-of-Systems" Processor (11:30)

M. B. Doerr
Coherent Logix, Inc., Austin, TX

Many Department of Defense (DoD) signal-processing systems must operate on vast amounts of data, requiring immense computational speed in a compact very-low-power device. A revolutionary new programmable and dynamically reconfigurable, networked, processor architecture, HyperX™, has been shown to provide orders of magnitude better computing performance and energy efficiency than any programmable processor available today. In collaboration with tri-Service system developers, DARPA, and the DoD Trusted Foundry program, the first HyperX™ is being fabricated and benchmarked. A description of this chip and the DoD-sponsored applications will be presented.

LUNCH (12:00–1:30)

Session 24

SPACE APPLICATIONS II

Thursday, March 23 / 10:30 am – 12:00 pm / Room 3

Chair: **Ken Hunt**
AFRL/VSSE Kirtland AFB, NM

Co-Chair: **Charles Barnes**
Jet Propulsion Laboratory, Pasadena, CA

24.1: Application-Dependent Qualification of FPGAs (10:30)

D. Sheldon, G. Burke, and Y. Chen
Jet Propulsion Laboratory, Pasadena, CA

The uses of FPGA devices continue to increase in spacecraft missions and payloads. These devices make use of some of the most advanced CMOS processing technologies available. Qualification of these devices has become increasingly more challenging as the technology continues to shrink, while providing for ever-increasing feature capability. An integrated matrix approach to qualifying these FPGA devices will be provided. In particular, the role of device technology and its related qualification and reliability risks to design and application-dependent parameters will be discussed. Experimental results designed to reveal dependences of possible timing-related failures to core logic modules will be discussed.

24.2: Radiation Effects on Optoelectronic Devices in Space Missions (10:50)

A. Johnston
Jet Propulsion Laboratory, Pasadena, CA

Radiation degradation of optoelectronic devices will be discussed, including effects on optical emitters, detectors, and sensors. Failures of optoelectronics in fielded space systems will also be discussed, along with testing and qualification methods.

24.3: Applying Commercial Microelectronics in Deep-Space Spacecraft Missions (11:10)

G. Swift
Jet Propulsion Laboratory, Pasadena, CA

Radiation and reliability issues for commercial microelectronic applications in space will be discussed. Examples are included from long-duration missions, including single-event upset in DRAMs used in solid-state recorders, and resets caused by transients in power systems.

24.4: High-Voltage Electronics Radiation and Reliability Issues for Long-Term Space Missions (11:30)

L. Scheick, R. Chavez, M. Elgefari, and L. Selva
Jet Propulsion Laboratory, Pasadena, CA

In recent years, space missions have been employing designs that have required higher and higher voltages. The major radiation and reliability issues for high-voltage space applications as well as recent data related to radiation testing of power devices will be reviewed. The data includes, but is not limited to, silicon power diodes, MOSFETs, BJTs and IGBTs, and silicon carbide diode and switches. Finally, new design solutions on the part and system level to address the high-voltage issues will be presented.

LUNCH (12:00–1:30)

Session 25

MICROWAVE PHOTONICS

Thursday, March 23 / 1:30 - 3:00 pm / Room 1

Chair: **Keith Williams**
Naval Research Laboratory, Washington, DC

Co-Chair: **Gerald M. Borsuk**
Naval Research Laboratory, Washington, DC

25.1: **Microwave Photonics: A Technology and Capabilities Overview** **(1:30)**

K. Williams
Naval Research Laboratory, Washington, DC

An overview of microwave photonics, including current application utility/benefits and challenges for advanced system concepts will be presented. It will provide a review of component technology currently available, including recent developments and future development trends and needs.

25.2: **Ultra-Stable Coherent laser Oscillator** **(1:50)**

Y. Shevy
Orbits Lightwave, Inc., Pasadena, CA

A breakthrough "virtual ring" laser oscillator has been developed. The all-fiber laser emits greater than 100 mW and boasts an unprecedented S/N ratio, ultra-low AM and FM noise, and high-absolute-frequency stability.

25.3: **High-Performance High-Reliability Custom Dual InGaAs Photodiodes for 2–18-GHz Electronic-Warfare (EW) Applications** **(2:10)**

A. M. Joshi, D. R. Mohr, A. Rumyantsev, and S. Lemke
Discovery Semiconductors, Ewing, NJ

Custom dual InGaAs photodiodes using our proprietary dual-depletion region (DDR) technology have been developed. The devices demonstrate high reliability and superior rf performance, thus making them ideal for deployment in the field by services such as the U.S. Navy.

25.4: **A Hybrid Packaging Approach for Highly Integrated Photonics** **(2:30)**

G. J. Whaley, B. L. Uhlhorn, J. A. Krawczak, and K. J. Thorson
Lockheed Martin, Eagan, MN

The development of an advanced multichannel DWDM fiber-optic receiver will be described. Hybrid integration is used to combine a fiber input to an athermal AWG, coupled to a pin photodiode array and simultaneous drive of a transimpedance amplifier array chip all housed in a single package.

BREAK **(3:00–3:30)**

Session 26

NANOTECHNOLOGY FOR SYSTEMS I

Thursday, March 23 / 1:30 – 3:10 pm / Room 2

Chair: **Cliff Lau**
Institute for Defense Analysis, Alexandria, VA

Co-Chair: **Joe E. Brewer**
University of Florida, Melrose, FL

26.1: **Self-Organized Quantum-Dot Architectures: Platforms for Next-Generation Sensing, Processing, and Communication Technologies** **(1:30)**

A. Madhukar
University of Southern California, Los Angeles, CA

Epitaxial self-organized quantum dots provide a manufacturable platform for the next generation of sources (LEDs, lasers), detectors (photo- and biochemical), optical amplifiers, and computing elements integrable into electronic, optoelectronic, and photonic systems with significantly enhanced performance.

26.2: **CMOL: Silicon's Chance for Reincarnation** **(2:10)**

K. Likharev
SUNY at Stony Brook, Stony Brook, NY

Recent work on prospective hybrid semiconductor/nanowire/nanodevice ("CMOL") integrated circuits, including an evaluation of their possible performance in applications such as terabit-scale memories, reconfigurable digital logic circuits, and mixed-signal neuromorphic networks will be reviewed.

26.3: **Low-Power High-Speed Carbon-Nanotube Field-Effect Transistors for Defense rf Electronics** **(2:50)**

H. Zhang, A. A. Pesetski, J. E. Baumgardner, and J. M. Murduck
Northrop Grumman, Linthicum, MD

A 23-GHz carbon-nanotube (CNT) field-effect transistor (FET) was demonstrated. This is a 40x improvement in maximum operating frequency and the highest operating frequency for CNT-FETs reported to date. It presents a significant breakthrough in the realization of carbon-nanotube-based electronics for low-power high-frequency applications.

BREAK **(3:10–3:30)**

Session 27

PHOTONICS AND ITS APPLICATION FOR COMPUTING AND SENSING

Thursday, March 23 / 3:30 – 5:00 pm / Room 1

Chair: **Michael D. Gerhold**
U. S. Army Research Office, Research Triangle Park, NC

Co-Chair: **Jony Jiang Liu**
U.S. Army Research Laboratory, Adelphi, MD

27.1: **A Compact Multifiber Single-Mode Expanded-Beam Fiber-Optic Connector Using In-Situ Self-Formed Polymer Waveguides** **(3:30)**

G. J. Whaley
Lockheed Martin, Eagan, MN

K-L. Deng, T. Gorczyca, and B. Lee
General Electric Co., Niskayuna, NY

A new high-density MT-style single-mode fiber-optic connector is under development which uses expanded beams to reduce the effects of particulate contamination. The connector incorporates a beam-expanding waveguide chip and an in-situ self-formed array of polymer waveguides to connect the chip to the fiber pigtail array.

27.2: **Design and Implementation of a Tactical Free-Space Optics Link to a UAV Using COTS Components** **(3:50)**

A. M. Cordes, R. L. Nelson, and R. C. Stevens
Lockheed Martin, Eagan, MN

The design and implementation of a high-bandwidth low-cost optical link between a UAV and a ground station will be described. System requirements are a 1-Gbps link at over 1 km, with a UAV payload weight of less than 15 lb.

27.3: **Optical Interconnect Loop-Back Switch for In-Situ Diagnostics** **(4:10)**

O. Blum Spahn
Sandia National Laboratories, Albuquerque, NM

K. Thorson and C. Kryzak
Lockheed Martin, Eagan, MN

G. Forman
General Electric Global Research Center, Niskayuna, NY

A novel solution for fiber-optic-link diagnostics has been developed through a collaborative effort between Lockheed Martin, Sandia National Laboratories, and General Electric to create a novel solution to fiber-optic-link diagnostics. The optical development provides tactical aircraft an in-situ optical network health by providing loop-back.

27.4: Opportunities for Fiber-Optic Networks in Military Avionics (4:30)

B. L. Uhlhorn, R. C. Stevens, and G. J. Whaley
Lockheed Martin, Eagan, MN

Military avionics has yet to fully realize the potential of fiber optics. This is partly due to the extreme environmental challenge, but also because typical systems requirements fall outside typical Datacom and Telecom specifications. Several opportunities in military avionics where fiber optics may provide significant benefit will be described.

Session 28

NANOTECHNOLOGY FOR SYSTEMS II

Thursday, March 23 / 3:30 – 5:30 pm / Room 2

Chair: **Cliff Lau**
Institute for Defense Analysis, Alexandria, VA

Co-Chair: **Joe E. Brewer**
University of Florida, Melrose, FL

28.1: Carbon-Nanotube Transistors for Digital Circuits (3:30)

A. Raychowdhury and K. Roy
Purdue University, West Lafayette, IN

Carbon-Nanotube transistors have gained immense popularity as future channel material for transistors. Models of carbon-nanotube FETs (CNFETs), suitable for circuit simulations, will be presented. These models are used to gauge the circuit and system-level performance of CN-FETs for ultra-scaled technologies.

28.2: Chemical Detection Using a Single-Walled Carbon-Nanotube Network Sensor (4:10)

E. Snow, K. Perkins, and S. Stepnowski
Naval Research Laboratory, Washington, DC

E. Houser
TSA, Atlantic City, NJ

A chemical detector based on a SWNT sensor that is fed by a micro-machined vapor delivery system is being developed. The detector can be customized for a range of vapors including CWAs, TICs, and explosives.

28.3: Carbon Nanotubes with Magnetic Particle Fillings as Nano-Electromechanical Systems (NEMS) (4:50)

A novel NEMS structure based on a supra-molecular structure consisting of a carbon nanotube containing freely moving nano-spheres of magnetic material will be presented. Preliminary theoretical and experimental studies will be discussed. This type of NEMS may potentially be able to operate in the gigahertz range.

H. Xin
University of Arizona, Tucson, AZ

J. Leonard and C. Bailey
Raytheon Missile Systems, Tucson, AZ

Q. Jiang
University of California, Riverside, CA

28.4: Molecular Micro-Switches for Reconfigurable X- and Ka-Band Apertures (5:10)

D. K. Brock, J. W. Ward, R. F. Smith, and B. M. Segal
Nantero, Inc., Woburn, MA

Molecular micro-switches, constructed from monolayers of carbon nanotubes, offer an option to conventional MEMS devices for reconfigurable rf and optical apertures. Unlike MEMS elements, these lithographically created molecular devices can be treated as lumped elements well into the multi-GHz range. The significance of this feature will be described for several existing phased-array aperture approaches.

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